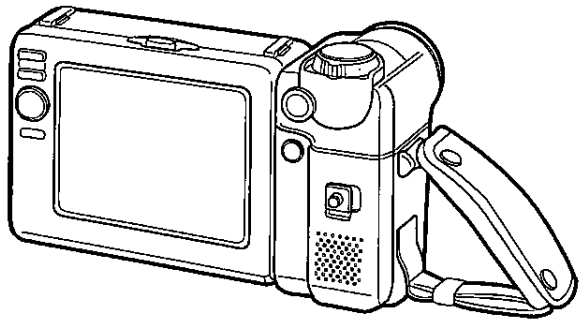
SHARP TECHNICAL MANUAL

T68S2VL-DC3U/

LIQUID CRYSTAL DIGITAL VIDEO CAMERA



Mini DV SHARP VIEWCAM

VL-DC3U/UT
VL-DC3S/H/E

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SHARP CORPORATION

1. OUTLINE OF PRODUCT

ADVANTAGES OF VL-DC3 SERIES

1. 4"(10.1cm) monitor mounted, size and weight reduction realized

The 4"(10.1cm) wide screen LCD monitor which ensures easy photographing and easy watching in the playback mode is provided, and the unique rotation tilt mechanism is applied. Owing to high degree integration of main LSIs of record/playback system and application of high-density mounting technology for components the thickness and weight were reduced remarkably, so that the machine can be easily carried by hand. Long time photographing and high angle photographing are facilitated.

2. Continuous long time recording (about 120 minutes)

Owing to reduction of power consumption of unit and application of the new high capacity battery it is possible recording continuously for about 120 minutes, using one battery.

3. Proposal of new uses with digital system expansion

The combination with the optional still unit (VR-SU3 or VR-3SUP for PAL) makes it possible to use the machine as a digital still camera or for digital optical communication (IrDA) which does not need wire connection, and allows the digital connection(*) to the personal computer and printer. The machine is provided with the digital output terminal (conforming to IEEE1394) which supports the digital signal communication. Video signal and audio signal are output as digital signals. It enables the digital transfer in which picture quality deterioration occurs scarcely. In the future it will be used as digital moving picture output terminal for the personal computer.

* Communication with the personal computer needs the specified digital still picture transfer software VR-PK31.

4. Adaptable to diversified playback digital effect function

The machine is provided with the playback effect function, utilizing the 4"(10.1cm) wide screen LCD monitor.

- It is possible to magnify the playback picture up to 4 times. Besides it is provided with the playback zoom function to move the magnification center to the left or right or up or down. One picture can be played back variously.
- The machine is provided with the overall playback function to overlap the second picture on the still picture.

5. Other advantages

(1) × 25 (× 10 optical) digital variable speed zoom

(VL-DC3E : × 40 (× 10 optical))

(2) High quality picture frame still (record and playback) ensuring clear reproduction of fine parts of still picture

(3) High picture element and wide visual field angle LCD monitor adopted

(4) The LCD guide operation button ensuring operation without changing the holding hand during photographing is provided.

(5) Instantaneous zoom magnifying by 1.5/2/2.5 times with one button

(VL-DC3E: 4.0 times)

(6) High sound quality 32 kHz 12-bit PCM stereo recording/after-recording

(7) Frame unit indicating time code

(8) Digital blur correcting system

NEW OPTIONS

The following optional attachments are marketed newly.

1. Still unit (VR-SU3:NTSC model or VR-3 SUP:PAL model)

When the still unit is connected to the VL-DC3 series, the VIEWCAM serves as a digital still camera. Since it uses the digital optical communication (IrDFA), digital communication with personal computer is enabled without wire connection.

Advantages

(1) High picture quality frame still

As the main unit ensures high picture quality frame still (*1), high resolution still picture 720 × 480 (702 × 480 when fetched in personal computer) has been realized in unit.

*1 High quality frame still with least blur is realized by detecting the motion part from 2 field pictures and subsequently synthesizing. (The motion part has the resolution of the field.)

(2) Tape index playback function provided

The start part of picture or title part is searched from the picture recorded on the tape and fetched into the still unit, and the picture is displayed wholly (16 divisions). The 16-division display allows the user to check the content of tape and find the tape top.

(3) Multi-mode function provided

The decorative frame can be attached to the picture. In combination with optional digital color printer (VP-EC1) the user enjoy the 16-division seal print.

(4) Application for personal computer with specific software

Fetching of digital still picture, album editing/processing, bi-directional communication, seamless synthesis (creation of panorama picture)(*2) are enabled by using the specified digital still picture transfer software.

*2 Windows95 only

New technology of camera section

High quality picture frame still recording

Motion to each picture element is detected in the direction of time axis from two field still pictures, and two pictures are synthesized. The vertical resolution of motionless part (still part) is 2 times higher than that of conventional field still, so that high quality still picture with least blur is obtained.

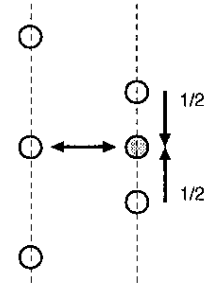
Technical point

Increase of detection accuracy of moving picture element (3:1 interpolation system)

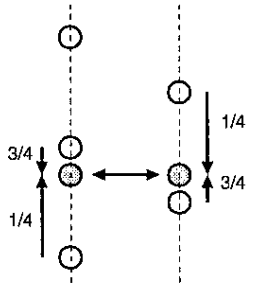
If pictures of two fields are compared as they are to detect the motion between two fields, the simple comparison does not give correct result because data do not exist in the same position due to interlace scan.

The new system is designed as follows. The data for comparison are made from the fields A and B, and the new algorism is used to compare them. Thereby the accuracy of motion detection is remarkably improved. Accordingly, the motion part and still part are accurately divided.

3:1 interpolation system



Conventional system



○ Field
◎ Comparison position

Ultrasmall light weight technology

1. Increase of density of main LSIs

The LSI for DVC has been newly developed, and the CSP package has been adopted for part of them, so that the PWB mounting area has been remarkably reduced as compared to the conventional LSI system for DVC.

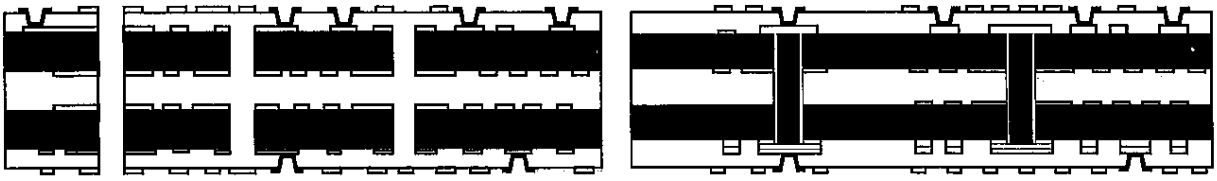
	Conventional LSI system	Newly developed LSI system
Design process	0.5μm or 0.6μm	0.35μm or 0.5μm
Number of chips	10 pcs.	5 pcs.
(Number of CSPs used	–	2 pcs.)
LSI area	about 3,200mm²	about 1,400mm²

(About ▲56%)

2. High density mounting technology

So as to increase the density of PWB we have adopted the Via on Via specification build-up PWB first in the industry, so that the component occupation rate (83%) and wiring density (72 pins/cm^2) was improved. As a result of reduction of components and application of CSP the single main PWB has been realized in place of conventional dual PWB. As a result the thickness of circuit unit was reduced from 13.1 mm to 6.2 mm (reduction by 6.9 mm), so that the thickness of product was reduced.

(General 6-layer build-up PWB) **(Via on Via type 6-layer build-up PWB)**



Reduction of thickness of tilt unit: The thickness of tilt unit was reduced from 11.5 mm to 9.5 mm (3 divisions of FPC in place of 2 divisions, reduction of FPC width).

3. Reduction of size of LCD section

So as to reduce the thickness of LCD section we have developed the lamp and light guide plate.

	Sharp's conventional LCD	Newly developed LCD
Thickness of LCD section	10.4mm	7.7mm
Lamp diameter	Φ2.6	Φ2.0
Thickness of light guide	4.0mm	3.0mm
Lamp type	Semi-hot	Cold cathode

So as to improve the luminance the following measures have been taken.

① Application of newly developed reflection polarizer: The light utilization efficiency has been improved by about 30%

② Optimization of color filter of LCD panel: The transmissivity has been improved by about 10%. As a result the luminance has been improved (as compared to the Sharp's former models of LCDs)

Backlight, light: Approx. 20%

Backlight, ordinary: Approx. 10%

4. Weight reduction technology

(1) Improvement of tilt mechanism frame

Material change

Because the magnesium containing aluminum alloy has been adopted, the thickness was reduced from 0.8 mm to 0.6 mm without reduction of strength, so that the mass has been reduced (by 3.7%).

(2) Adoption of external appearance metallic parts

① Reduction of heat radiation and shield parts

As a result of improvement of heat radiation effect and shield effect due to application of metal cabinet the heat radiation parts and shield parts have been reduced (by about 30 g)

② Reduction of cabinet thickness

As a result of increase of rigidity and strength due to application of metal cabinet the thickness of cabinet has been reduced.
(Plastic 1.1 mm ➡ Aluminum 0.8 mm)

Digital system

As the digital system has been applied to the LCD Viewcam, we propose the new uses where its advantages are utilized effectively.

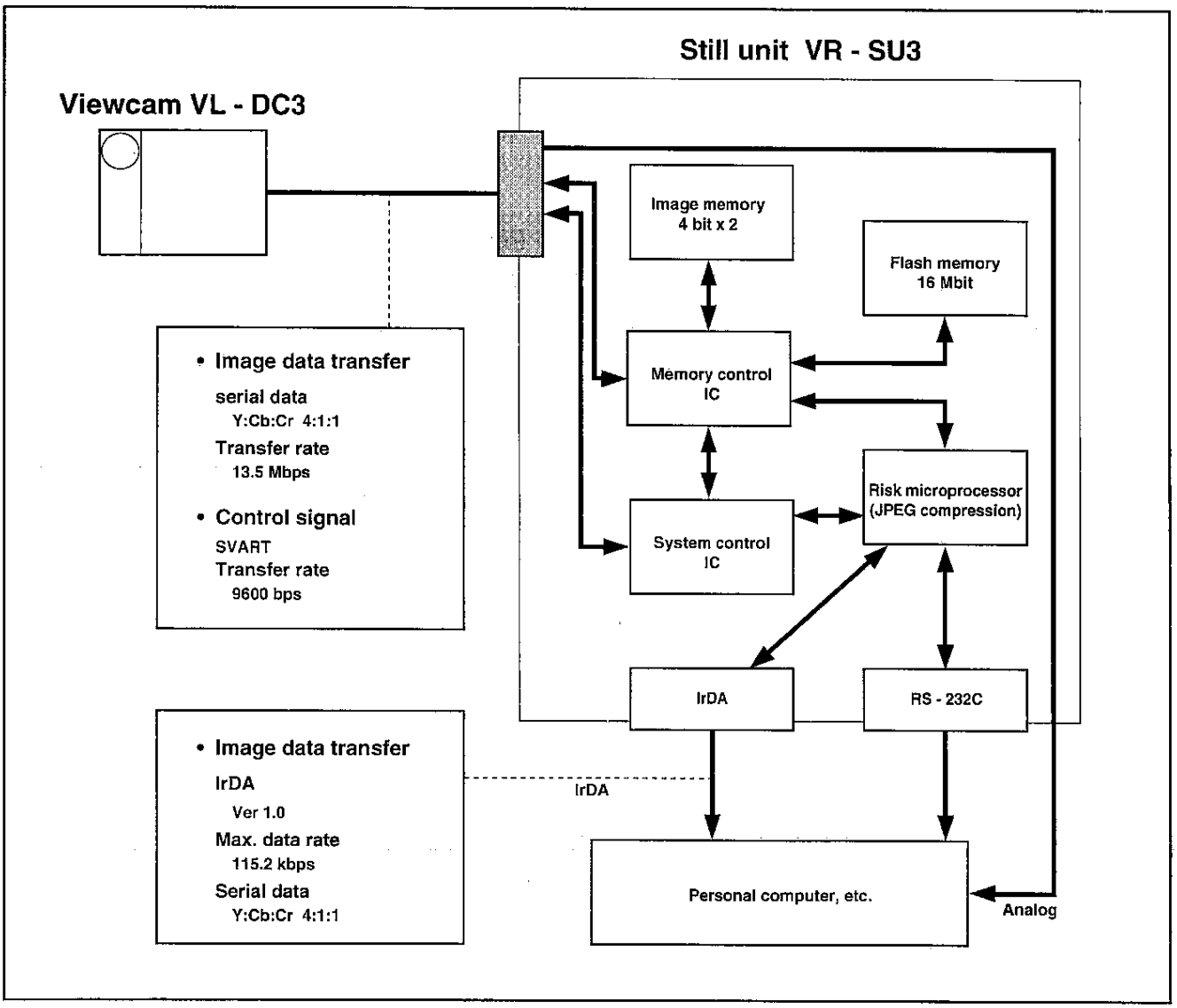
① Still photographing

The still picture is stored in the flash memory. The machine performed the functions of VCR and still camera.

② Digital communication

The high quality digital communication using the personal computer has been realized.

Block diagram



Still unit expansion function

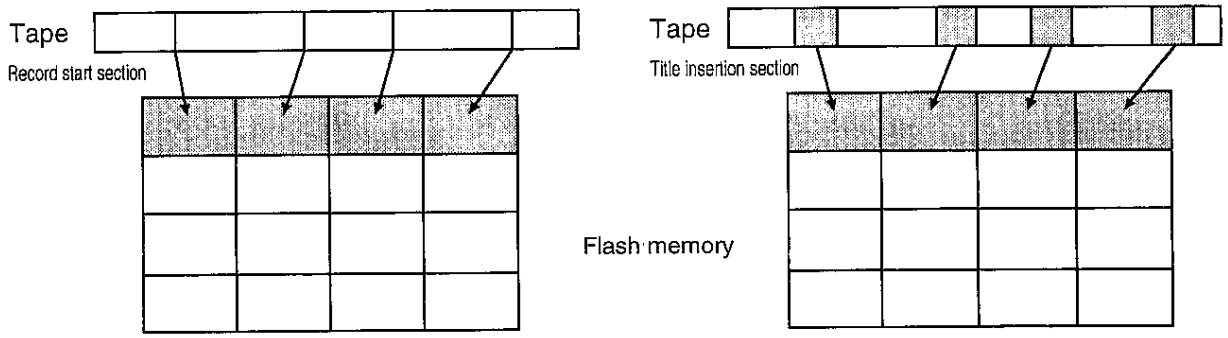
Tape index function

The function to display the record start section or title insertion photographing (the still picture of still unit is put at the top of moving picture to use it as a title) on the LCD monitor as a list (16 divisions). It is possible to check the content of tape or to find at once the required scene from it.

Construction

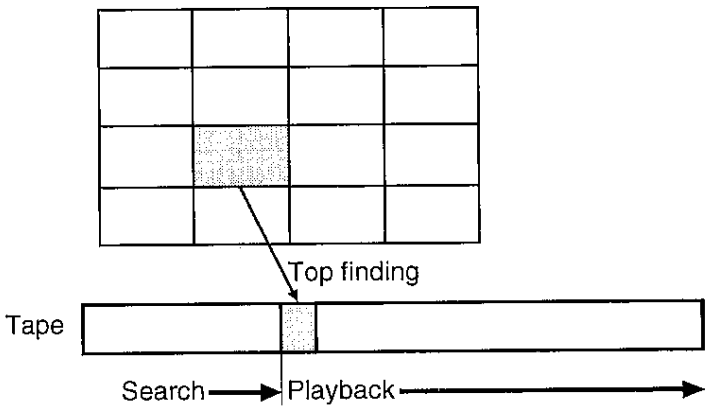
(1) When the record start section is selected to find the top

(2) When the title is selected to find the top



The record start section or title insertion section (snap/still photographing) is fetched in the flash memory as thumbnail picture while the tape search is performed. When 16 screens are read, 16-division screen appears. At this time the data code corresponding to each picture is recorded in the flash memory.

When a required picture is selected from the 16-division screen, top finding is started herefrom.



Personal computer software

Explanation of seamless synthesis technology

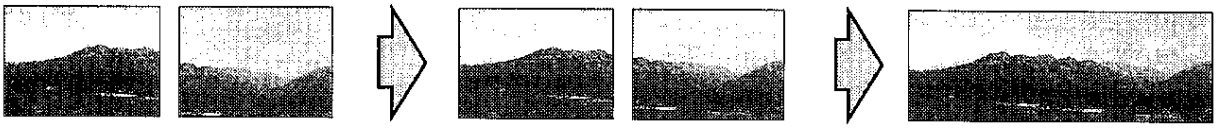
(digital still picture transfer software VR-PK31 PIXLABO)

The seamless synthesis is a function to synthesize seamless continued picture and to convert it into a still picture. It is possible to make long panorama, using the photograph taken with the VIEWCAM. When photographing one still picture containing extremely small letters, take photograph, dividing it into several parts, and then combine them (synthesize) so that the high definition still picture can be made with readable letters.

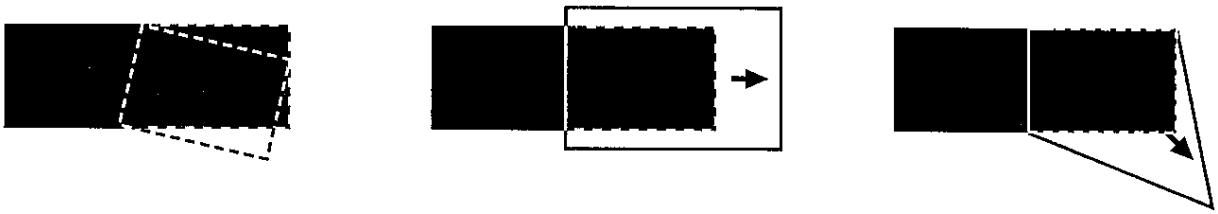
Take the required part from the moving picture tape taken with the VIEWCAM, and record it as a still picture in the still unit to perform seamless synthesis.
(You can make a grand panorama photograph, using some tape!)

Explanation of seamless synthesis function

(1) In case of seamless synthesis the several still pictures are aligned.



(2) The insignificant difference of profiles of overlapping parts and luminance (due to lens strain or exposure in case of photographing) is adjusted by rotation, magnification, reduction, deformation and luminance adjustment.



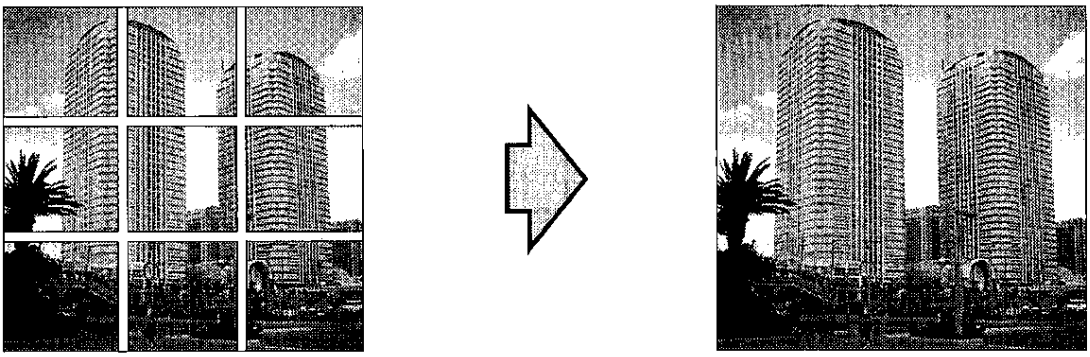
Uses of seamless synthesis

Panorama synthesis

To make the still picture showing grand scenery or big building for catalog or home pages which cannot be expressed with the ordinary camera.

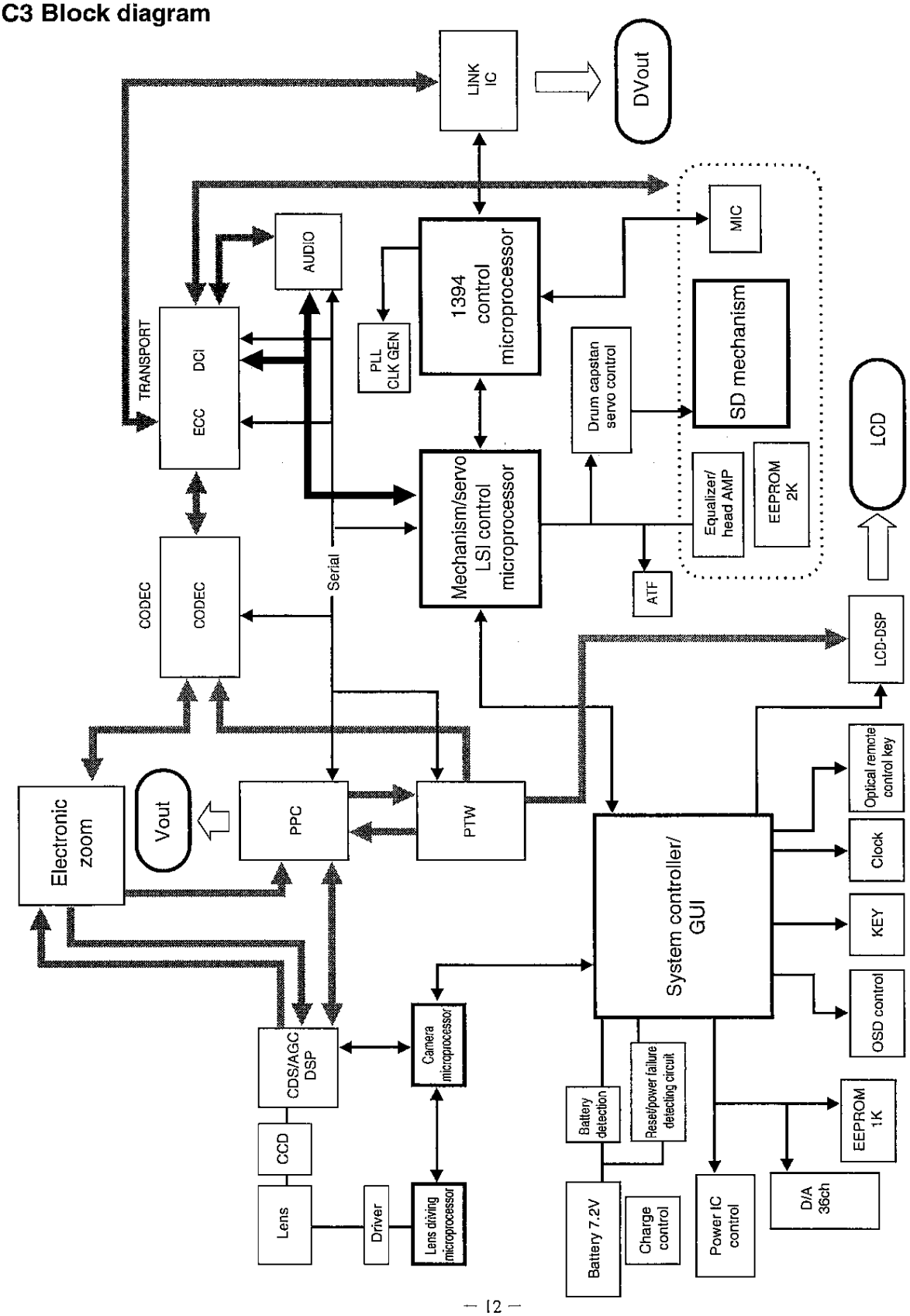
High picture quality systnesis

Several photographs are combined vertically and horizontally. 4-piece synthesis corresponds to 1,000,000 pixels, and 8-piece synthesis corresponds to 2,500,000 pixels. Still picture of higher resolution can be made by increasing the number of component pieces.

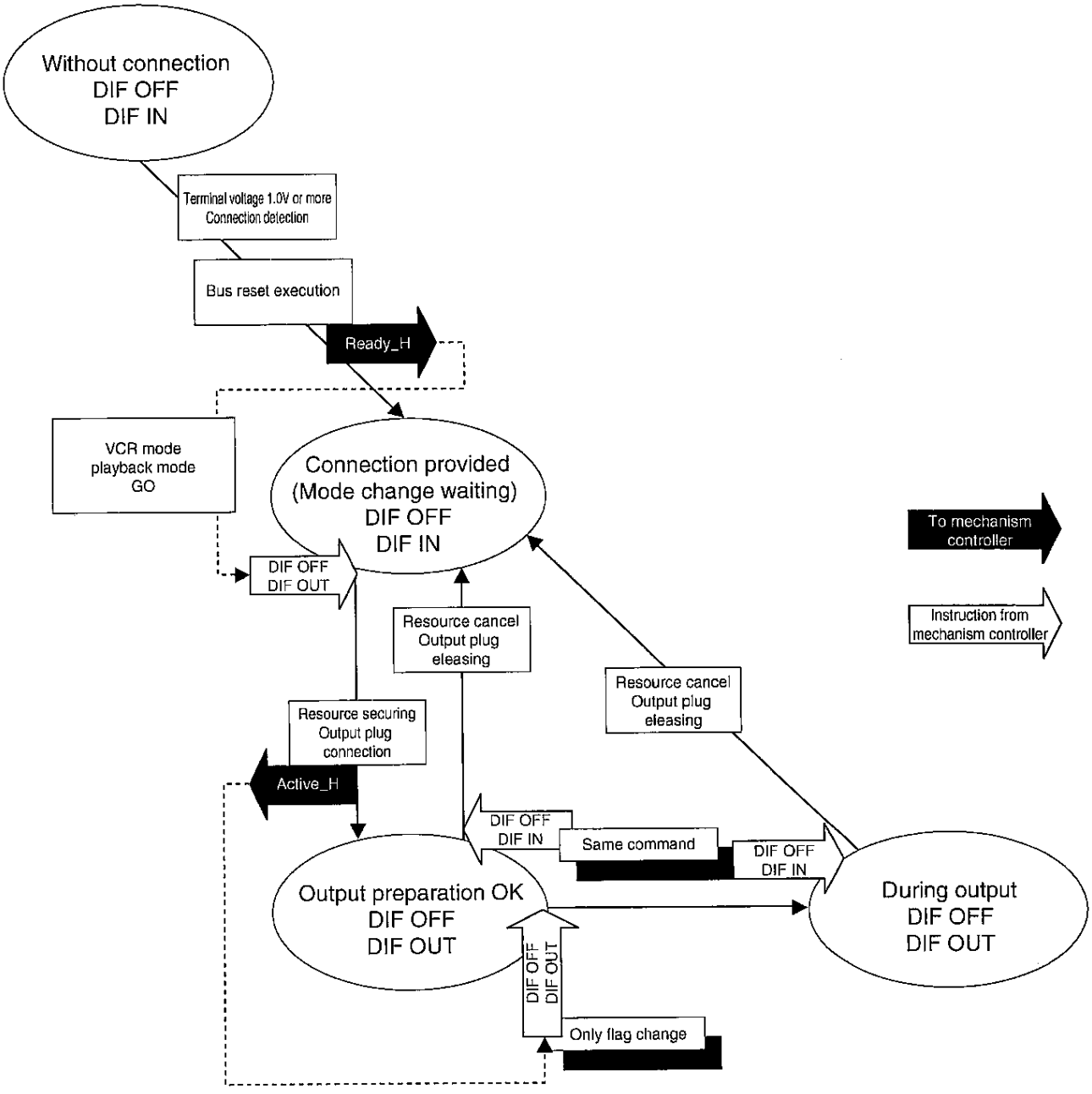


2. GENERAL SIGNAL PROCESSING

■DC3 Block diagram



■1394 microprocessor mode change diagram



3. CAMERA CIRCUIT

High picture quality frame still

Until now the field picture was used to fetch the still picture. This caused the problem of degradation of vertical resolution as compared to ordinary picture. The frame still using the simple 2 fields improved the resolution of still part but caused the problem of degradation of picture quality of moving part. Recently we have developed a new system of still picture technology to solve these problems.

1. Outline

Motion is detected from the two field pictures, and correction is made to create one blurless high quality picture.

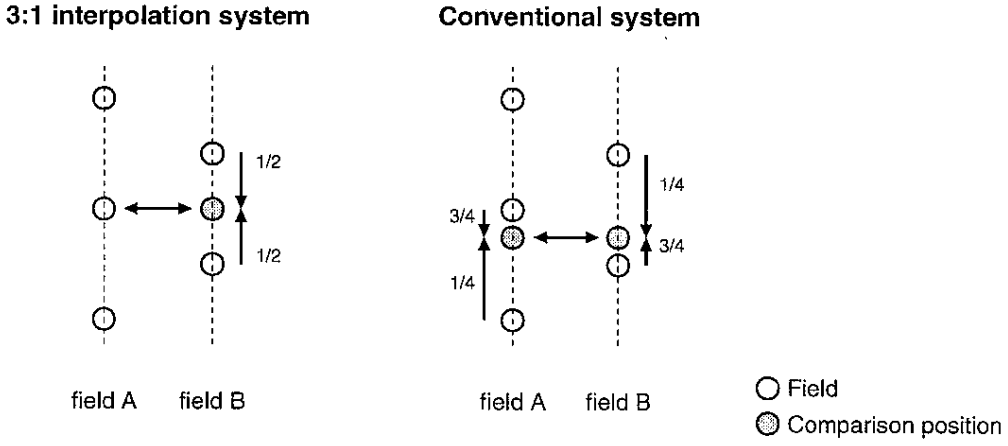
Moving picture element: In-field interpolation
Still picture element: In-frame interpolation

2. Technical point

(1) Motion/still picture element separating technology

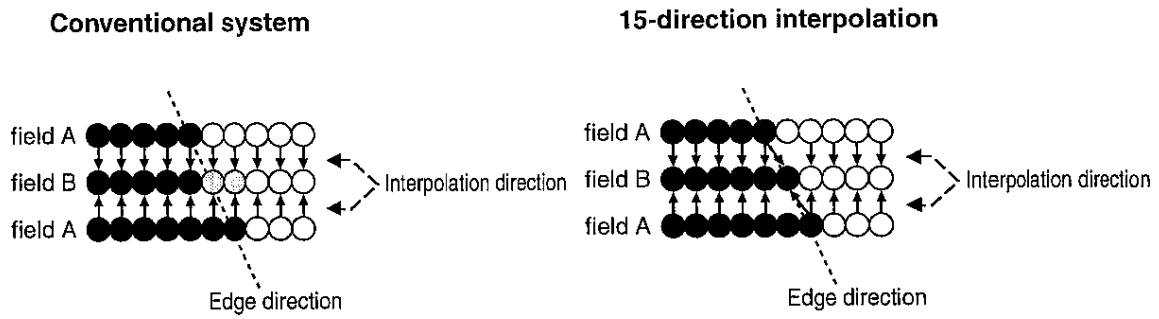
If an attempt is made to compare the pictures of 2 fields to detect the moving picture element of two fields, the samples comparison does not give the correct result because data does not exist in the same position due to interlace scan. Applying the new algorithm, we have solved this problem so as to ensure correct separation of motion area and still area.

Data for comparison is created from the field A and field B, and these data are compared, so that the accuracy of motion detection is remarkably improved. (3:1 interpolation system)



(2) Half-picture element accuracy 15-direction interpolation technology

After separation of moving picture element and still picture element by motion detection the in-field interpolation is applied for the moving picture element. Generally the average of upper and lower picture elements is taken. If this method is applied, the diagonal line and curved line appear unsmooth. We have developed the algorithm to interpolate along the predicted edge direction, so that the smooth edge can be obtained.

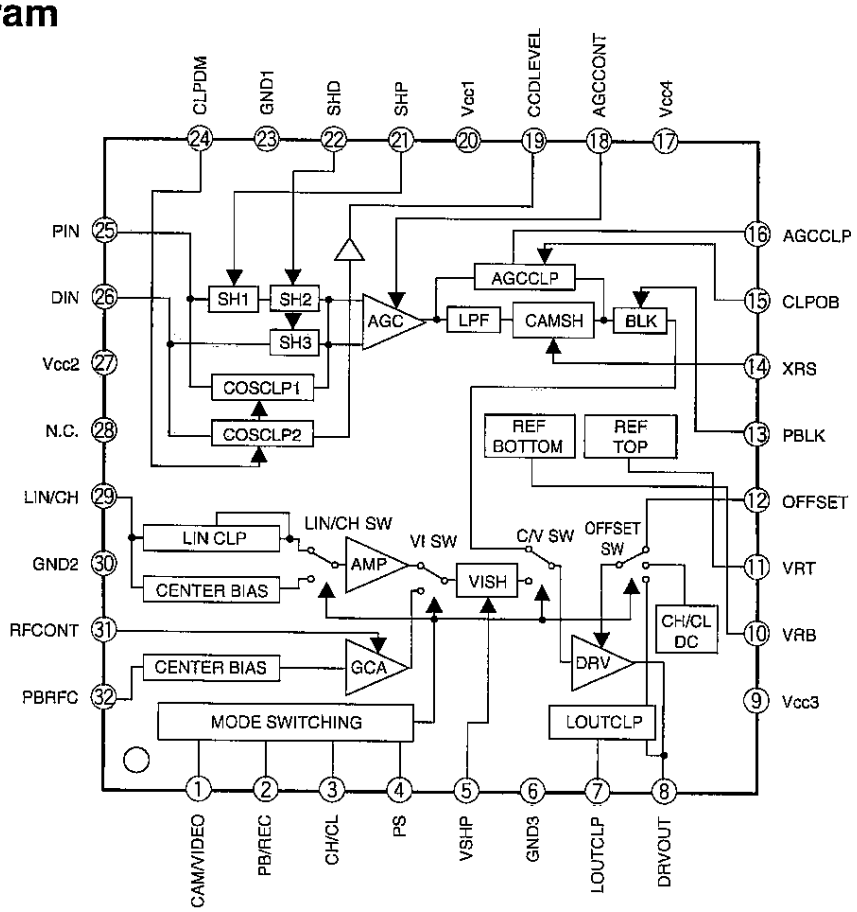


Conclusion

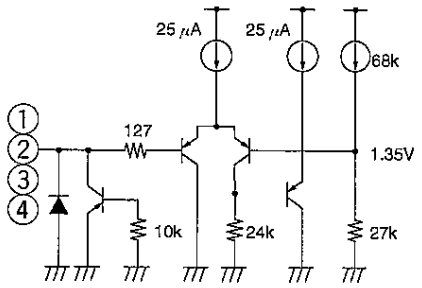
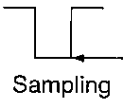
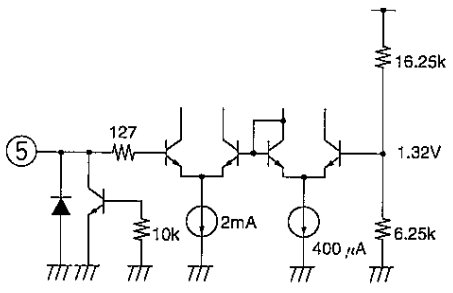
While the whole screen does not move, the frame still is applied to the whole screen. If part of screen is moving, in-field interpolation still is applied to only this part. If the whole screen is moving, the in-field interpolation still is applied. In combination with the 15-direction interpolation the new system ensures remarkable improvement of picture quality.

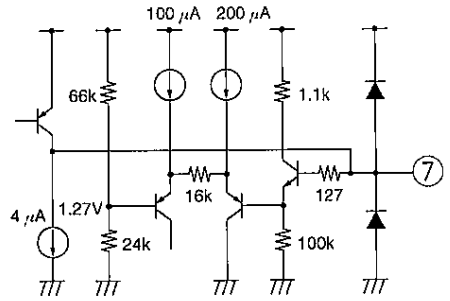
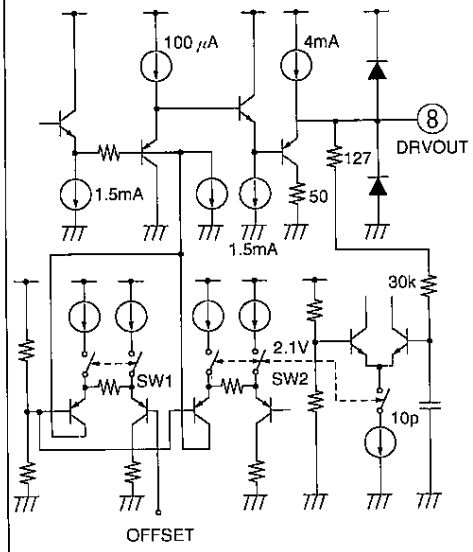
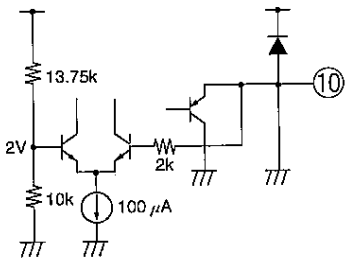
IC block diagram(IC101)VHiCXA2006Q-1

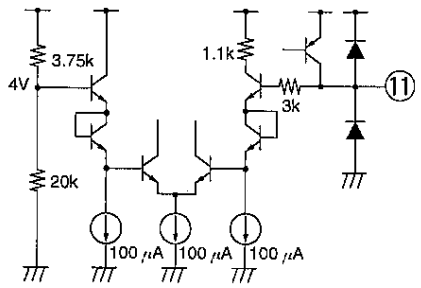
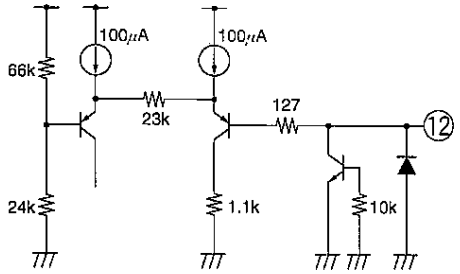
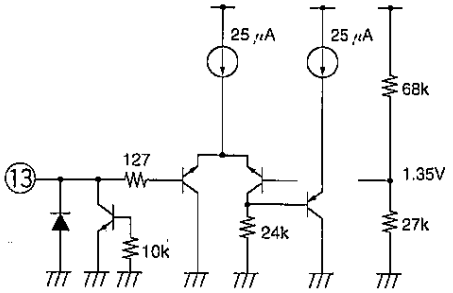
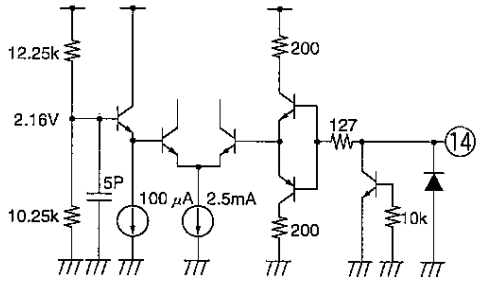
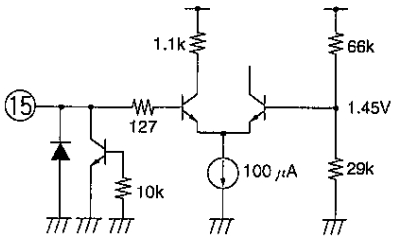
1. Block diagram

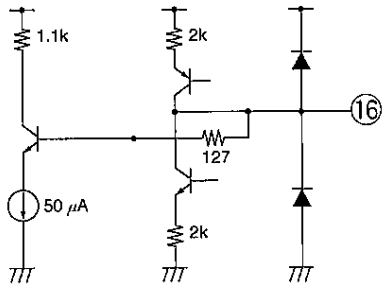
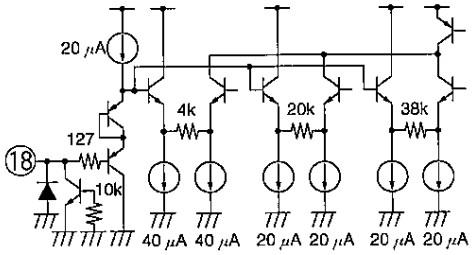
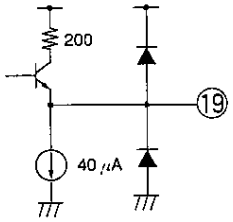
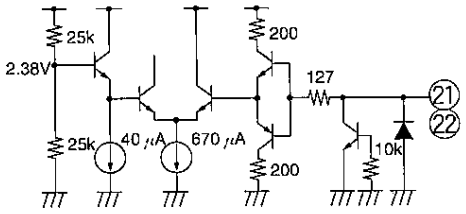
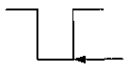
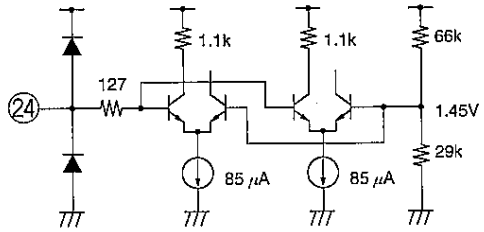


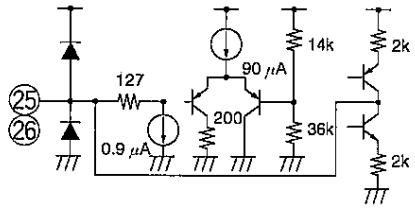
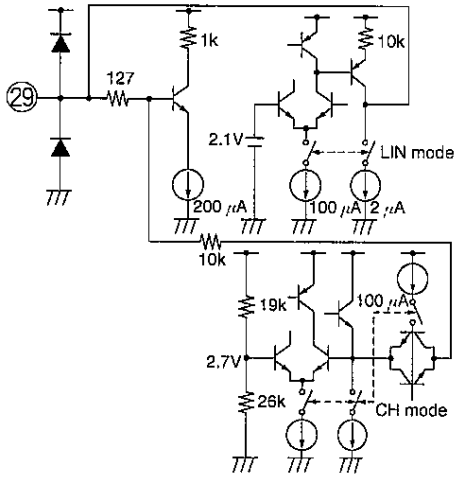
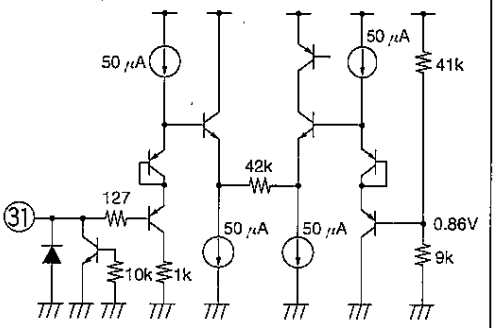
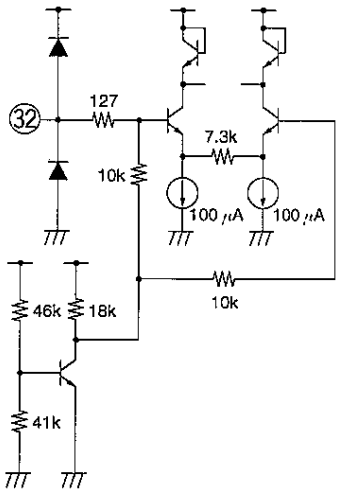
2. Explanation of terminal

Terminal No.	Terminal mark	Terminal voltage	Equalizing circuit	Explanation of terminal
1	CAM/ VIDEO	VTH = 1.35V		Camera and video signal switching terminal
2	PB/REC			Chroma signal and composite video signal switching terminal
3	CH/CL			High range chroma signal and low range chroma signal switching terminal
4	PS			Power save mode terminal
5	VSHP	Sampling VTH = 1.32V  Sampling		Video sample hold pulse input terminal

<table>
<tr><th>Terminal No.</th><th>Terminal mark</th><th>Terminal voltage</th><th>Equalizing circuit</th><th>Explanation of terminal</th></tr>
<tr><td>6
23
30</td><td>GND3
GND1
GND2</td><td>GND</td><td></td><td>Grounding terminal</td></tr>
<tr><td>7</td><td>LOUTCLP</td><td>About 2V</td><td> 
</td><td>Terminal to connect the capacitor for LOUTCLP to clamp the minimum level of output in the mode where composite video (Recommended value: 0.1μF)</td></tr>
<tr><td>8</td><td>DRVOUT</td><td>• Camera mode (CAM)
VRB – 200mV
Black level
VRB –300mV
• Composite video mode(LIN)
VRB +100mV
• Chroma mode(CH, CL)
Intermediate point voltage = (VRT – VRB) / 2</td><td> 
</td><td>Signal is passedDriver output terminal for A/D converter enabling DC direct connection
Dynamic range = 2Vpp
<table><tr><th>SW1</th><th>SW2</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>CH,CL</td></tr><tr><td>0</td><td>1</td><td>CAM</td></tr><tr><td>1</td><td>0</td><td>LIN</td></tr><tr><td>1</td><td>1</td><td>—</td></tr></table>0 : Close
1 : Open</td></tr>
<tr><td>9
20
27</td><td>Vcc3
Vcc1
Vcc2</td><td>Vcc</td><td></td><td>Power terminal</td></tr>
<tr><td>10</td><td>VRB</td><td>2.0V</td><td> 
</td><td>2V regulator output terminal</td></tr>
</table>

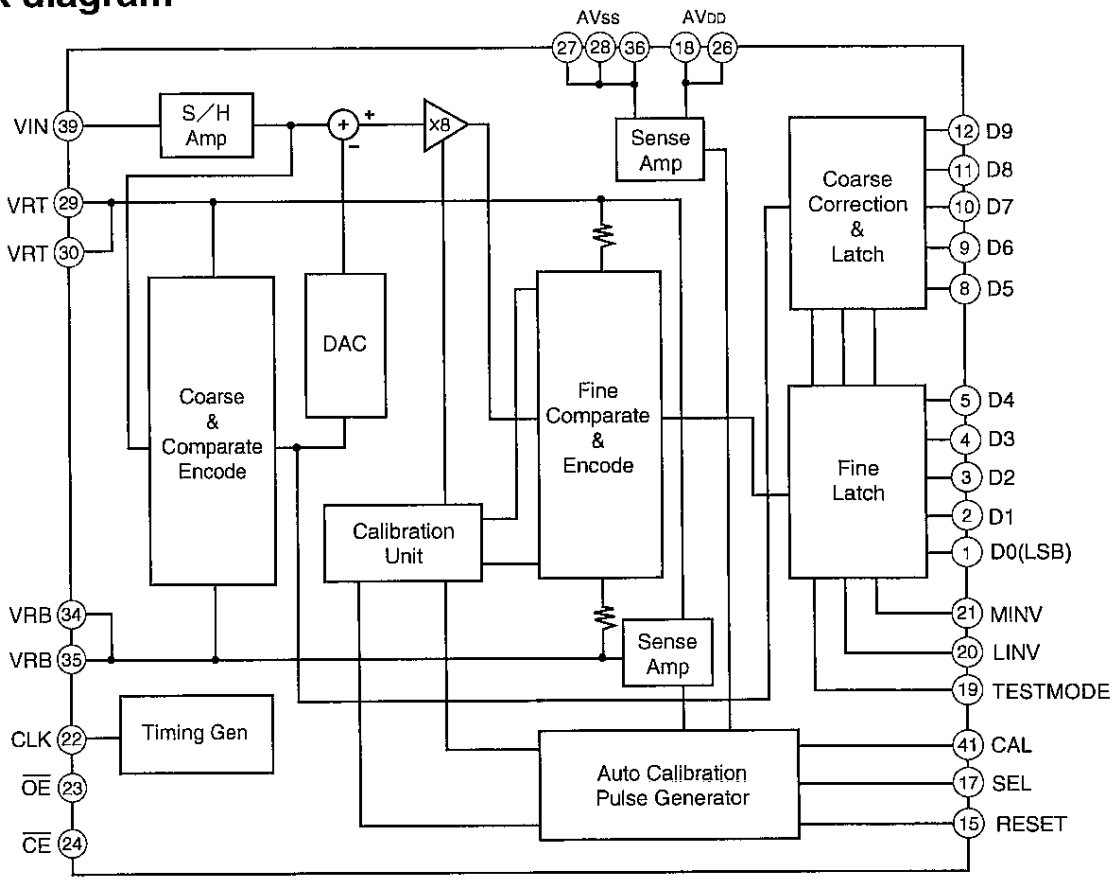
Terminal No.	Terminal mark	Terminal voltage	Equalizing circuit	Explanation of terminal
11	VRT	4.0V		4V regulator output terminal
12	OFFSET	0.8 ~ 3V		Terminal to control output offset in camera mode 0.8V : (VRT - 200 mV) or less 3.0V : (VRT + 300 mV) or more
13	PBLK	VTH = 1.35V Active : Low		Camera signal preblanking pulse input terminal It functions at Low only in the camera mode. Calibration of black level of AGC output waveform is performed. When PBLK = Low, the potential of DRVOUT is forcibly set to 2V.
14	XRS	VTH = 2.16V Sampling		Camera signal sample hold pulse input terminal Clamp pulse terminal to clamp the optical black part of camera signal after passing of AGC amplifier
15	CLPOB	VTH =1.45V Active : Low		Clamp pulse terminal to clamp the optical black part of camera signal after passing of AGC amplifier

Terminal No.	Terminal mark	Terminal voltage	Equalizing circuit	Explanation of terminal
16	AGCCLP	About 3V		AGC clamp Condenser for (Recommended value: 0.1 uF)
17	Vcc4			Nonconnection Ordinary grounding
18	AGCCONT	0.8 ~ 3V		AGC gain control terminal 0.8V: 8 dB (MIN gain) 3.0V: 38dB (MAX gain)
19	CCDLEVEL	DIN input CCD signal black level About 2.7V		Terminal allowing monitoring SHD output camera signal
21	SHP	VTH = 2.38V		Sample hold pulse input terminal for preset level
22	SHD	 Sampling		Sample hold pulse input terminal for data level
24	CLPDM	VTH = Low Active : Low		Clamp pulse terminal to clamp input CCD signal at dummy picture element

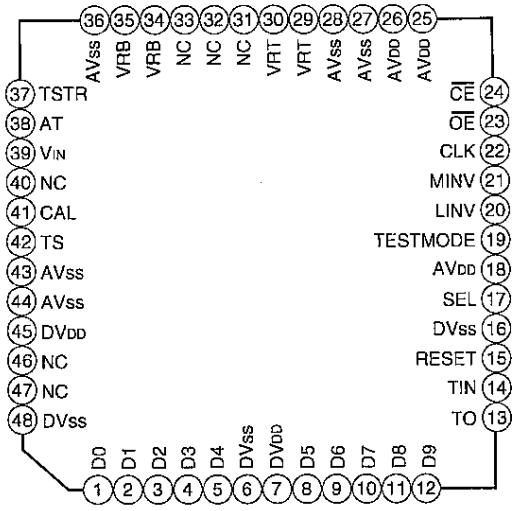
Terminal No.	Terminal mark	Terminal voltage	Equalizing circuit	Explanation of terminal
25 26	PIN DIN	Black level About 2.7V		CCD signal input terminal
29	LIN/CH	LIN mode clamp potential About 2.4V CH mode About 2.7V		Composite video signal (LIN) and high range chroma signal (CH) common-use input terminal
31	RFCONT	0.8 ~ 3V		Gain control terminal for low range chroma signal (CL) 0.8V: 8 dV (MIN gain) 3.0V: 38dB (MAX gain)
32	PBRFC	About 2.94V		Low range chroma signal (CL) input terminal

(IC151)VHiCXD2310A-1

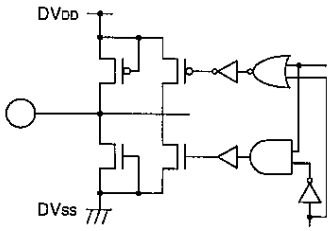
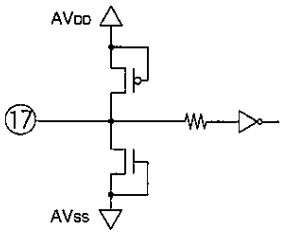
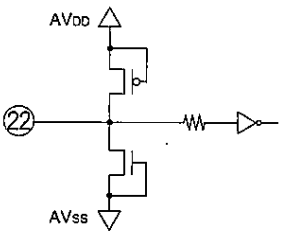
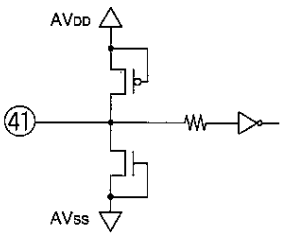
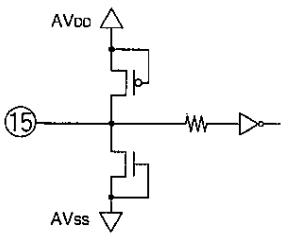
1. Block diagram

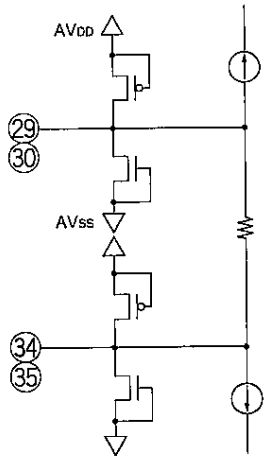
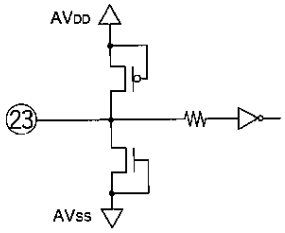
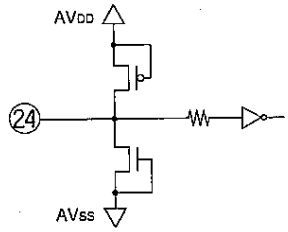
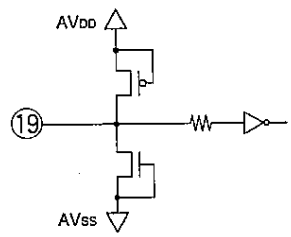


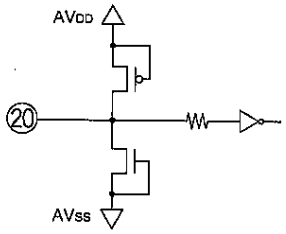
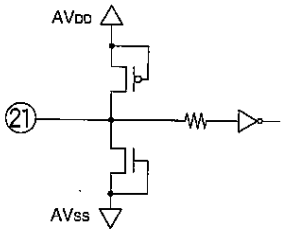
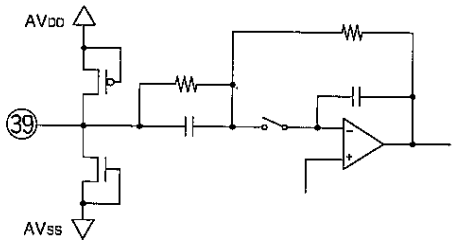
2. Terminal Arrangement



3. Explanation of terminal

Terminal No.	Terminal mark	Equalizing circuit	Explanation of terminal
1 ~ 5 8 ~ 12	D0 ~ D9		D0(LSB)~D9(MSB) Output
13	TO		Test terminal Ts = High: High impedance
7, 45	DVDD		Digital VDD
6, 16, 48	DVSS		Digital Vss
27, 28, 36, 43, 44	AVSS		Analog Vss
17	SEL		Calibration input pulse selection terminal (after completion of startup calibration) High:Generation of internal pulse Low: External input
22	CLK		Clock terminal
41	CAL		Calibration pulse input terminal
15	RESET		Calibration circuit reset and startup calibration restart terminal

Terminal No.	Terminal mark	Equalizing circuit	Explanation of terminal
14	TIN		Test signal input terminal To be fixed usually to AVDD or AVss
29, 30	VRT		Reference top terminal
34, 35	VRB		Reference bottom terminal
38	AT		Test signal output terminal TS = High: High impedance state
42	TS		Test signal input terminal To be fixed usua lly to AVDD
37	TSTR		Test signal input terminal To be fixed usually to AVDD or AVss
23	$\overline{OE}$		Output (D0 to D9) enable terminal Low: Output state High: High impedance state
24	$\overline{CE}$		Chip enable terminal Low: Operating state High: Standby state
19	TESTMODE		Test mode terminal High: Output state Low: Fixed output

Terminal No.	Terminal mark	Equalizing circuit	Explanation of terminal
20	LINV		Test mode terminal High: D0 to D8 is inverted and output.
21	MINV		Output inversion terminal High: D9 is inverted and output.
18, 25, 26	AVDD		Analog VDD
39	VIN		Analog input terminal

4. Function operation

4-1 Function operation (IC12) VHiLR385117/-1

No.	Mark	I/O	Polarity	Terminal name	Function
1	V1X	03	⎍	Vertical transfer pulse output 1	Pulse output terminal to drive the vertical CCD shift register #1 of area sensor To be connected to the 1AX input terminal of vertical driver IC.
2	V2X	03	⎍	Vertical transfer pulse output 2	Pulse output terminal to drive the vertical CCD shift register #2 of area sensor To be connected to the 2AX input terminal of vertical driver IC.
3	V3X	03	⎍	Vertical transfer pulse output 3	Pulse output terminal to drive the vertical CCD shift register #3 of area sensor To be connected to the 3AX input terminal of vertical driver IC.
4	V4X	03	⎍	Vertical transfer pulse output 4	Pulse output terminal to drive the vertical CCD shift register #4 of area sensor To be connected to the 4AX input terminal of vertical driver IC.
5	OFDX	03	⎍	OFD pulse output	Terminal to output the pulse to remove charges when the electric shutter operates. Superposition on area sensor OFD voltage through inversion voltage increasing circuit Normal mode: H level output.
6	GND	–	–	Grounding terminal	Grounding
7	VDD3	–	–	Power	+2.7V is supplied.
8	VH1X	03	⎍	Charge read pulse output 1	Terminal to output the pulse to transfer the charge of area sensor photodiode to the vertical CCD shift register #1. To be connected to the 1BX input terminal of vertical driver IC.
9	VH3X	03	⎍	Charge read pulse output 3	Terminal to output the pulse to transfer the charge of area sensor photodiode to the vertical CCD shift register #3. To be connected to the 1BX input terminal of vertical driver IC.
10	MR1	ICU3	–	Phase control input R1	Input terminal to control the fall of area sensor reset pulse FR (terminal 20) in case of building-up of FH1 (terminal 40). The pulse width can be changed insignificantly.
11	MR2	ICU3	–	Phase control input R2	
12	MC1	ICU3	–	Phase control input C1	Input terminal to control the phase of FCX pulse (terminal 18) in case of fall of FH1 (terminal 40), being used together with MC2 (terminal 48) Phase difference.

MR-1	H	L	L	H
MR-2	H	H	L	L
Pulse width	A	A+a	A+2a	A+3a

Simulation value [Type]
A ; 16ns (Note 1)
a ; 1.5ns

MR-1	H	L	L	H
MR-2	H	H	L	L
Phase	A	A+a	A+2a	A+3a

Simulation value [Type]
A ; -2.5ns (Note 1)
a ; 1.5ns

No.	Mark	I/O	Polarity	Terminal name	Function
13	PBLX	05	⊓	Preblanking pulse output	Terminal to output the pulse to apply the blanking to the area sensor signal. Horizontal period continuous pulse.
14	BCPX	05	⊓	Optical black clamp pulse output	Terminal to output the pulse to clamp the optical black for each horizontal line of area sensor. Composite pulse which gets L level while effective picture element does not exist during vertical blanking period.
15	CLPX	–	⊓	Clamp pulse output	Terminal to output the clamp pulse to clamp the area sensor dummy output. Horizontal period continuous pulse.
16	GND	–	–	Grounding terminal	Grounding
17	FSX	06 MA5	⊓	CDS pulse output 2	Terminal to output the pulse to sample-hold the area sensor output signal. The phase in case of building-up of FH1 (terminal 40) can be changed insignificantly with MS1 (terminal 37) and MS2 (terminal 38).
18	FCX	06 MA5	⊓	CDS pulse output 1	Terminal to output the clamp pulse to clamp quickly the area sensor output signal. The phase in case of fall of FH1 (terminal 40) can be changed insignificantly with MC1 (terminal 12) and MC2 (terminal 48).
19	RSX	06 MA5	⊓	Sample hold pulse output	Terminal to output the pulse to sample-hold after CDS/AGC operation at CDS/AGC-IC. Pulse phase is fixed.
20	FR	06 MA52	⊔	Reset pulse output	Terminal to output the pulse to reset the charge of area sensor output circuit. To be connected to (R of area sensor through DC offset circuit. The building-up of FR in case of building-up of FH1 (terminal 40) is fixed (simulation value [typ.]; 0ns), but the phase of fall can be changed insignificantly with MR1 (terminal 10) and MR2 (terminal 11).
21	VDD5	–	–	Power	+5V is supplied.
22	MF1	ICU5	–	Phase control input F1	Input terminal to control the phase of RSX pulse (terminal 19) in case of fall of FSX (terminal 17) The pulse phase can be changed insignificantly.
23	MF2	ICU5	–	Phase control input F2	<table><tr><td>MR-1</td><td>H</td><td>L</td><td>L</td><td>H</td></tr><tr><td>MR-2</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>Phase</td><td>A</td><td>A+a</td><td>A+2a</td><td>A+3a</td></tr></table> Simulation value [Type] A ; -2.5ns (Note 1) a ; 1.5ns
24	CLP	05	⊔	Clamp pulse output	Terminal to output the reverse polarity (positive polarity) pulse of CLPX (terminal 15) output.
25	CKI	0SCI 3	⊓⊓	Clock input	Reference clock input terminal It and CDO (terminal 26) compose the oscillation circuit. Since it is not provided with resistor, fit the feedback resistor. NTSC system: 28.63636 MHz, 1820 fH PAL system: 28.37500 MHz, 1816 fH (fH: one horizontal period)
26	CKO	0SC0 3	⊓⊓	Clock output	Inversion output terminal of CKI (terminal 25)

<table>
<tr><th>No.</th><th>Mark</th><th>I/O</th><th>Polarity</th><th>Terminal name</th><th>Function</th></tr>
<tr><td>27</td><td>CLK</td><td>06
MA3</td><td> </td><td>1/2 frequency-division output</td><td>Terminal to output 1/2 frequency-division continuous pulse of reference clock CKI (terminal 25). It is synchronized with fall of CKI.
NTSC system : 14.31818 MHz, 910 fH
PAL system : 14.18750 MHz, 908 fH (fH: one horizontal period)</td></tr>
<tr><td>28</td><td>HD</td><td>IC3</td><td> </td><td>Horizontal reference input</td><td>Timing IC horizontal reference signal input terminal. The negative polarity horizontal reference pulse is supplied from SSG-IC.</td></tr>
<tr><td>29</td><td>VD</td><td>IC3</td><td> </td><td>Vertical reference input</td><td>Timing IC vertical reference signal input terminal. The negative polarity reference pulse is supplied from SSG-IC.</td></tr>
<tr><td>30</td><td>VDD3</td><td>–</td><td>–</td><td>Power</td><td>+2.7V is supplied.</td></tr>
<tr><td>31</td><td>GND</td><td>–</td><td>–</td><td>Grounding terminal</td><td>Grounding</td></tr>
<tr><td>32</td><td>ED0</td><td>ICD3</td><td>–</td><td>Shutter control 1</td><td rowspan="3">Electronic shutter speed control input terminal (No.2)</td></tr>
<tr><td>33</td><td>ED1</td><td>ICD3</td><td>–</td><td>Shutter control 2</td></tr>
<tr><td>34</td><td>ED2</td><td>ICD3</td><td>–</td><td>Shutter control 3</td></tr>
<tr><td>35</td><td>TVMD</td><td>ICD3</td><td>–</td><td>TV mode selection input</td><td>Input terminal to select TV system
<table><tr><td>TVMD</td><td>L</td><td>H or open</td></tr><tr><td>TV system</td><td>NTSC</td><td>PAL</td></tr></table></td></tr>
<tr><td>36</td><td>PWMD</td><td>ICU3</td><td>–</td><td>Power save mode selec tion input</td><td>Input terminal to fix pulse output (excepting CLK (terminal 27)) L level and to stop internal operation.
H level or open : Normal operation
L level : L level output excepting</td></tr>
<tr><td>37</td><td>MS1</td><td>ICU4</td><td>–</td><td>Phase control input S1</td><td rowspan="2">Input terminal to control the phase of FSX (terminal 17) in case of building-up of FH1 (terminal 40).
The pulse phase can be changed insignificantly.
<table><tr><td>MR-1</td><td>H</td><td>L</td><td>L</td><td>H</td></tr><tr><td>MR-2</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>phase</td><td>A</td><td>A+a</td><td>A+2a</td><td>A+3a</td></tr></table>Simulation value [Type]
A ; -2.5ns (Note 1)
a ; 1.5ns</td></tr>
<tr><td>38</td><td>MS2</td><td>ICU4</td><td>–</td><td>Phase control input S2</td></tr>
<tr><td>39</td><td>GND</td><td>–</td><td>–</td><td>Phase grounding</td><td>Grounding</td></tr>
<tr><td>40</td><td>FH1</td><td>06MA
44</td><td> </td><td>Horizontal transfer pulse output 1</td><td>Terminal to output the pulse to drive the area sensor horizontal CCD shift register #1.
To be connected to area sensor ΦH1.</td></tr>
<tr><td>41</td><td>VDD4</td><td>–</td><td>–</td><td>Power</td><td>+3.6V is supplied.</td></tr>
<tr><td>42</td><td>FH2</td><td>06MA
44</td><td> </td><td>Horizontal transfer pulse output 2</td><td>Terminal to output the pulse to drive the area sensor horizontal CCD shift register #2.
To be connected to area sensor ΦH2.</td></tr>
<tr><td>43</td><td>GND</td><td>–</td><td>–</td><td>Grounding terminal</td><td>Grounding</td></tr>
</table>

No.	Mark	I/O	Polarity	Terminal name	Function
44	N. C.	–	–	(Empty terminal)	Without internal wiring
45	VDD4	–	–	Power	+3.6V is supplied.
46	TEST	ICD4	–	Test input	Input terminal for test. Usually open or set to L level.
47	PSMD	ICD4	–	Data input system selection input	Input terminal to select the electronic shutter speed setting data input (note 2) H level : Parallel data input mode L level or open : Serial data input mode
48	MC2	ICU4	–	Phase control input C2	Input terminal to control the phase of FCX pulse (terminal 18) in case of fall of FH1 (terminal 40), being used together with MC1 (terminal 12) Phase difference.

Note 1: The simulation value is type. value in the case where clock of duty 50% is input into CKI (terminal 25).
Note 2: Refer to the shutter control table.

4-2 Terminal arrangement (IC502)RH-IX0546TAZZ DC3 CAM Terminal

No.	Terminal name	Terminal function name	I/O	Explanation	To be connected to:
1	P32/SCK0	SIO CLK LENS	I	Serial clock from lens microcomputer	lens microcom.
2	P33/SO0/SB0	CAM TO LENS	O	Serial data to be transferred to lens microcomputer	lens microcom.
3	P34/T00	LENS READY	O	READY signal output to lens microcomputer	lens microcom.
4	P35/T01	BURE RESET	O	Blur detection IC reset signal ("L": Reset)	
5	P36/T02	BURE PWR DWN	O	Blur detection power-down control output	
6	P37/T03	LENS RESET	O	LOW: Resetting of lens microcomputer ▲2/20	
7	RESET	RES	I	Reset input	
8	Vdd	VCC		2.8V power (min 2.7V)	
9	X2	XTAL	I	16MHz X'tal Connection terminal	
10	X1	EXTAL	I	16MHz X'tal Connection terminal	
11	Vss	GND			
12	P00	IRMODE	O	IRDA input/output selection mode	ZOOM DSP
13	P01	AD PS	O	HIGH: Camera AD power saving (HIGH is set when external REC COMP signal is input.)	CAMERA A/D
14	P02	CAM/PB_CTL	O	Zoom IC playback mode control (Playback: HIGH) ▲2/20	ZOOM DSP
15	P03	CAM H1	O	CAM mode: HIGH (3-state buffer selection) ▲2/20	
16	P04	STILL LOW	O	LOW output only when STILL unit is connected. ▲2/20	
17	P05	SLOW CTL 1	I	Reverse slow control signal 1 from mechanism controller	mechanism controller
18	P06	SLOW CTL 2	I	Reverse slow control signal 2 from mechanism controller	mechanism controller
19	P07	SLOW CTL 3	I	Reverse slow control signal 3 from mechanism controller	mechanism controller
20	P67/REFREQ/HLDAK	PB BURE H1	O	HIGH: Only playback blur occurs ▲2/20	ZOOM IC
21	P66/WAIT/HLDRQ	NC	O	LOW output ▲2/20	
22	P65/WR	NC	O	LOW output	
23	P64/RD	NC	O	LOW output ▲2/20	
24	P63/A19	F1	I	Field index	ZOOM IC
25	P62/A18	NC	O	LOW output ▲2/20	SYSCON
26	P61/A17	NC	O	LOW output	
27	P60/A16	NC	O	LOW output	
28	P57/A15	DATA7/ADRS7	I/O	DSP/BURE Data/address input/output bit 7(parallel)	CAM/ZOOM
29	P56/A14	DATA6/ADRS6	I/O	DSP/BURE Data/address input/output bit 7 BIT6	CAM/ZOOM
30	P55/A13	DATA5/ADRS5	I/O	DSP/BURE Data/address input/output bit 7 BIT5	CAM/ZOOM
31	P54/A12	DATA4/ADRS4	I/O	DSP/BURE Data/address input/output bit 7 BIT4	CAM/ZOOM
32	P53/A10	DATA3/ADRS3	I/O	DSP/BURE Data/address input/output bit 7 BIT3	CAM/ZOOM
33	P52/A9	DATA2/ADRS2	I/O	DSP/BURE Data/address input/output bit 7 BIT2	CAM/ZOOM
34	P51/A8	DATA1/ADRS1	I/O	DSP/BURE Data/address input/output bit 7 BIT1	CAM/ZOOM
35	P50/A7	DATA0/ADRS0	I/O	DSP/BURE Data/address input/output bit 7 BIT0	CAM/ZOOM
36	P47/AD7	XPCK	O	DSP/BURE Bus data latch clock	CAM/ZOOM
37	P46/AD6	XPMODE	O	DSP/BURE Bus data/address selection("L" = DATA)	CAM/ZOOM
38	P45/AD5	XPR/W	O	DSP Bus data READ/WRITE selection("L" = active)	CAM DSP

No.	Terminal name	Terminal function name	I/O	Explanation	To be connected to:
39	P44/AD4	XPCS_DSP	O	DSP Bus chip selection ("L" = active)	CAM DSP
40	P43/AD3	XPCS_BURE	O	BURE chip selection ("L" = MOVING)	ZOOM IC
41	P42/AD2	BURE R/W	O	LSI bus data READ/WRITE selection ("L" = MOVING)	ZOOM IC
42	P41/AD1	NC	O	LOW output	ZOOM IC
43	P40/AD0	NC	O	LOW output	ZOOM IC
44	AST8/CLKOUT	NC			
45	Vss	GND		GND	
46	TEST	GND		GND	
47	P10/PWM0	NC	O	LOW output	
48	P11/PWM1	MEM_CTL	O	Frame: LOW Field: HIGH	ZOOM IC
49	P12/ASCK2/SCK2	TEST2	O	OSD CLK output (control of debug OSD)	
50	P13/RxD2/S12	TEST1	O	OSD CS output, RS-232C data input	
51	P14/TxD2/S02	TEST0	O	OSD DATA output, RS-232C data output	
52	P15	TEST3	O	Debug pulse output (land required)	
53	P16	ROM DATA	I/O	PWB E²PROM serial data input/output	E²PROM
54	P17	ROM CLK	O	PWB E²PROM serial clock output	E²PROM
55	Vdd	Vdd		2.8V(min2.7V)	
56	P70/AN10	CAM DSP RESET	O	LOW: Camera DSP resetting	CAM DSP
57	P71/AN11	NC	O	LOW output	
58	P72/AN12	NC	O	LOW output	
59	P73/AN13	NC	O	LOW output	
60	P74/AN14	NC	O	LOW output	
61	P75/AN15	NTSC/PAL	I	NTSC/PAL selection ("H" = PAL "L" = NTSC)	
62	P76/AN16	ADJ SW	I	Adjustment mode switch input	
63	P77/AN17	MODEL SEL	I	Model judgment (Europe/Australia/others) according to voltage	
64	AVdd	Avdd	I	Analog power (input of Vdd or less)	
65	AVref1	A/D REF	I	A/D reference voltage (AVref1 ≦ AVdd must be satisfied)	
66	AVss	GND			
67	AN00	Y GAIN	O	Buffer externally provided	OP AMP
68	AN01	C GAIN	O	Buffer externally provided	OP AMP
69	AVref2	Vdd	I	2.8V(min2.7V)	
70	AVref3	GND			
71	P20/NMI	GND	I	NMI "L" fixed	
72	P21/INTP0	DSP VD	I	VD input from CAM DSP	CAM DSP
73	P22/INTP1	TMNG	I	TMNG signal input terminal (from digital auto-LSI)	CAM DSP
74	P23/INTP2/C1	CFNSH	I	Blur detection operation end flag input (fall input)	ZOOM IC
75	P24/INTP3	READY	I	Serial transfer, READY input (common to system controller and automatic adjustment machine)	SYS MICON
76	P25/INTP4/SCK1	SIO CLK	O	Serial transfer clock output (common to system controller and auto matic adjustment machine)	SYS MICON
77	P26/INTP5	CODEC_VD	I	Input of VD from CODEC	CODEC
78	P27/SI0	LES TO CAM	I	Serial data from lens microprocessor	LNS MICON
79	P30/RxD/SI1	SYS TO CAM	I	Serial data from system controller	SYS MICON
80	P31/TxD/SO1	CAM TO SYS	O	Serial data from CAM microprocessor to system controller.	SYS MICON

*Resetting: All I/O ports are in high impedance state

4. MICROPROCESSOR E²PROM

Terminal arrangement

System controller (IC701)RH-IX0547TAN1

1. Terminal arrangement table (80VQFP 0.65 pitch, 14 mm square)

*1 State of port when power is off
*2 State of port in case of microprocessor resetting

No.	Terminal name	I/O	Type	*1	*2	Terminal function name	Explanation
1	ANO	I	Hi-Z	Z	Z	DEW	Dew detection A/D input
2	AVREF					Vcc	
3	AVcc					Vcc	VCC
4	PVcc					Vcc	VCC
5	PVss					Vss	GND VSS
6	P114/PWM0	O	CMOS	L	Z	SELECT - A	Terminal A for multiplexer input selection A /VDD
7	P115/PWM1	O	CMOS	L	Z	SELECT - B	Terminal A for multiplexer input selection B /SDA
8	P116/PWM2	O	CMOS	Z	Z	SELECT - C	Terminal A for multiplexer input selection C /SCK
9	P117/PEM3	O	CMOS	L	Z	PCON - H	VCR - Pcon - H
10	P67/INT6/W6	I	Hi - Z	Z	Z	BATT OFF	Power failure detection FSDA
11	P66/INT5/W5	I	Hi - Z	Z	Z	EJECT SW	Ejection FSCLK
12	P65/INT4/W4	I	Hi - Z	Z	Z	V - SYNC	FBUSY
13	P64/INT3/W3	I	Hi - Z	L	Z	M - PCON	System controller start terminal
14	P63/INT2/W2	I	Hi - Z	Z	Z	VCR SW	VCR power SW
15	P62/INT1/W1	I	Hi - Z	Z	Z	CAM SW	Camera power SW
16	P61/INT0/W0	I	Hi - Z	Z	Z	CASCON SW	Cassette controller switch
17	NMI	I	Hi - Z	L	Z	NMI	
18	XIN	I	Hi - Z	Z	Z	XIN	
19	IVss					IVSS	GND VSS
20	XOUT	O	CMOS	Z	Z	XOUT	
21	IVcc					IVCC	VCC
22	RESET	I	Hi - Z	Z	Z	RESET	RESET
23	MOD1	I	Hi - Z	Z	Z	MOD1	MOD1
24	MOD0	I	Hi - Z	Z	Z	MOD0	MOD0
25	P07/HLDA/WE	O	CMOS	Z	Z	A - CLK	
26	P06/HOLD/CE	O	Hi - Z	Z	Z	A - DATA	PLL free running control
27	P05/BLW	O	CMOS	L	Z	A - CS	
28	P04/BHW	O	CMOS	L	Z	NC	
29	P03/RD/OE	O	CMOS	L	Z	NC	OE
30	P02/BCLK	O	CMOS	Z	Z	NC	
31	P37/DC	I	Hi - Z	Z	Z	UP KEY IN	UP key input
32	P36/A30	I	Hi - Z	Z	Z	DOWN KEY IN	DOWN key input
33	P35/A29	I	Hi - Z	Z	Z	LEFT KEY IN	LEFT key input
34	P34/A28	I	Hi - Z	Z	Z	RIGHT KEY IN	RIGHT key input

No.	Terminal name	I/O	Type	*1	*2	Terminal function name	Explanation
35	P33/A27	I	Hi - Z	Z	Z	DISP KEY IN	Indication ON/OFF key input
36	P32/A26	I	Hi - Z	Z	Z	SELECT KEY IN	Indication selection key input
37	P31/A25	I	Hi - Z	Z	Z	REC S/S	REC Start / Stop SW
38	P30/A25	I	Hi - Z	Z	Z	TURN SW	
39	BVss					BVSS	GND VSS
40	BVcc					BVCC	VCC
41	IVcc					IVCC	VPP1
42	P27/A23	O	CMOS	L	Z	NC	
43	P26	O	CMOS	L	Z	NC	
44	P25	O	CMOS	L	Z	AV - H	
45	P24	O	CMOS	L	Z	NC	
46	P23	O	CMOS	L	Z	TUNE - H	
47	P22	O	CMOS	L	Z	NC	
48	P21	O	CMOS	L	Z	NC	
49	P20	I	CMOS	L	Z	SNAP	
50	IVcc					IVCC	VCC
51	IVss					IVSS	GND VSS
52	IVss					IVSS	GND VEE
53	P17	O	CMOS	L	Z	ADJ CTL	CAM automatic adjustment (HI: Adjustment)
54	P16	O	CMOS	L	Z	D/A STB	D/A data strobe
55	P15	O	CMOS	L	Z	D/A 1 H	D/A converter power
56	P14	O	CMOS	L	Z	AUDIO MUTE	Audio output control
57	P13	O	CMOS	L	Z	NC	1394 microprocessor READY Not used
58	P12	O	CMOS	L	Z	NC	1394 microprocessor CLOCK Not used
59	P11	O	CMOS	L	Z	NC	1394 microprocessor To system controller Not used
60	P10	O	CMOS	L	Z	NC	1394 microprocessor To microprocessor Not used
61	BVss					BVSS	GND VSS
62	BVcc					BVCC	VCC
63	Ivcc					IVCC	VPP2
64	P57	O	CMOS	L	Z	VIDEO RELS	Picture output control
65	P56	O	CMOS	L	Z	LINE SEL1	
66	P55	O	CMOS	L	Z	NC	
67	P54	O	CMOS	L	Z	LCLK	
68	P53	O	CMOS	L	Z	LMODE	
69	P52	O	CMOS	L	Z	LCS	
70	P51	I	Hi - Z	Z	Z	LRDY	
71	P50	I	Hi - Z	Z	Z	TEST - H	
72	P47	I/O	CMOS	Z	Z	LOAD0	LCD - DSP Parallel data 7
73	P46	I/O	CMOS	Z	Z	LOAD1	LCD - DSP Parallel data 6
74	P45	I/O	CMOS	Z	Z	LOAD2	LCD - DSP Parallel data 5
75	P44	I/O	CMOS	Z	Z	LOAD3	LCD - DSP Parallel data 4
76	P43	I/O	CMOS	Z	Z	LOAD4	LCD - DSP Parallel data 3
77	P42	I/O	CMOS	Z	Z	LOAD5	LCD - DSP Parallel data 2

No.	Terminal name	I/O	Type	*1	*2	Terminal function name	Explanation
78	P41	I/O	CMOS	Z	Z	LOAD6	LCD - DSP Parallel data 1
79	P40	I/O	CMOS	Z	Z	LOAD7	LCD - DSP Parallel data 0
80	MOD2	I	Hi - Z	Z	Z	MOD2	MOD2
81	P90/XCIN	I	Hi - Z	Z	Z	XCIN	Crystal connection terminal for clock Oscillation at 32 kHz
82	Ivss					IVSS	GND VSS
83	P91/XCOUT	O	CMOS	Z	Z	XCOUT	Crystal connection terminal for clock Oscillation at 32 kHz
84	IVcc					IVCC	VCC
85	P92	I	Hi - Z	Z	Z	REMOTE	IR remote control signal
86	P93	I	CMOS	L	Z	LCD RESET	
87	P94	I	CMOS	L	Z	E²PROM CS	Serial CS
88	P95	I	CMOS	L	Z	E²PROM D1	Serial data input
89	P96	I	CMOS	L	Z	NC	
90	P97	O	COMS	L	Z	NC	
91	P102	O	COMS	L	Z	OSD CLK	Clock to OSD-IC
92	P103	O	COMS	L	Z	OSD CS	Chip selection for OSD-IC
93	P104	O	COMS	L	Z	OSD DATA	Data for OSD-IC
94	P105	O	COMS	L	Z	NC	
95	P106	O	COMS	L	Z	PSC DATA	Common serial data
96	P107	O	COMS	L	Z	PSD CLK	Common serial clock
97	PVcc					PVCC	VCC
98	PVss					PVSS	GND VSS
99	P77	O	COMS	L	Z	CAM READY	Camera serial ready
100	P76	O	COMS	L	Z	CAM RESET	
101	P75	I	Hi - Z	Z	Z	CAM CLK	Serial clock from camera
102	P74	I	Hi - Z	Z	Z	CAM TO SYS	Serial data-in from camera
103	P73	O	COMS	Z	Z	SYS TO CAM	Serial data-out to camera
104	P87	O	COMS	L	Z	MEC READY	Mechanism control serial ready
105	P86	O	COMS	L	Z	MEC RESET	
106	P85	I	Hi - Z	L	Z	MEC CLK	Mechanism control serial clock
107	P84	I	Hi - Z	Z	Z	MEC TO SYS	Serial data-in to mechanism controller
108	P83	O	COMS	Z	Z	SYS TO MEC	Serial data-out to mechanism controller
109	P82	I	COMS	L	Z	DCCA L	DC cabled "L": Battery remaining capacity indication OFF
110	P81	I				SVART RXD	External equipment communication input
111	P80	O				SVART TXD	External equipment communication output
112	P72	O	COMS	L	Z	NC	
113	AVss					AVSS	GND VSS
114	AN7	I	Hi - Z	Z	Z	NC	GND (touch panel not used)
115	AN6	I	Hi - Z	Z	Z	NC	GND (touch panel not used)
116	AN5	I	Hi - Z	Z	Z	NC	GND (touch panel not used)
117	AN4	I	Hi - Z	Z	Z	ADJ - DET	Adjustment mode A/D input
118	AN3	I	Hi - Z	Z	Z	POWER CK	Power monitoring detection input A/D input
119	AN2	I	Hi - Z	Z	Z	ZOOM_SW	A/D input
120	AN1	I	Hi - Z	Z	Z	BATT	Battery voltage detection A/D input

2. D/A converter output terminal arrangement

36CH D/A Converter
(LCD/power system)

Terminal	Terminal name	Function	Description
38	A01	Backlight CTL1	Backlight 1 voltage control
39	A02	BL - ON	Backlight ON/OFF "H": ON
40	A03	ADJ DA-Y	PCO video output level ADJ
41	A04	ADJ DA-C	PCO video output level ADJ
42	A05		
43	A06	CAM +15V PCON	Camera + 15V Power control "H": ON
44	A07	CAM 4.9V PCON	Camera + 4.9V Power control "H": ON
45	A08	CAM 2.8V PCON	Camera + 2.8V Power voltage adjustment
46	A09	BL PWR	BL-PWR:H Backlight lights (PCON3, 1ADJ)
47	A10	COM BIAS ADJ	LCD common bias adjustment
48	A11	DAC_C_ADJ	
9	A12	W/B R ADJ	R white balance adjustment
10	A13	W/B B ADJ	B white balance adjustment
11	A14	DAC R ADJ	
12	A15	DAC_G_ADJ	
13	A16	DAC_B_ADJ	
14	A17	ATF F1 ADJ	ATF F1 frequency adjustment
15	A18	ATF F2 ADJ	ATF F2 frequency adjustment
16	A19	NC	
17	A20	THRESH 2 ADJ	Thresh level 2 ADJ (ATF, EQ/PLL)
18	A21	EQ TRANS ADJ	EQ transversal ADJ
19	A22	SEARCH-L	Video research "L" Usually "H"
20	A23	EQ_TAPE_SEL	EQ tape selection ME tape: "H" MP tape: "L"
21	A24	PLL FREERUN	PLL free run adjustment
22	A25	PLL OFFSETJ	PLL offset adjustment
23	A26	VCO ADJ	VCO frequency adjustment
24	A27	ATF - GAIN	
25	A28	PLL BIAS	CLKGEN PLL adjustment
26	A29	TU P - CON	Tuner power adjustment
27	A30	S2 - OUT	S2 output
28	A31	MIC/LINE	Microphone/LINE input selection
33	A32	FADE CTL	Audio fader output
34	A33	AV SEL	AV input/output priority selection Tuner: H
35	A34	VOL CTL	Sound volume control
36	A35	SP CTL	Speaker power control ON: "H"
37	A36	CAM L	Camera mode: "L"

3. Power IC serial control

Power IC is not used for VL-DC3.

4. Mechanism/servo terminal arrangement (100VQFP 0.5mm pitch)

*1 State of port in case of microprocessor resetting

No.	Terminal name	I/O	Type	*1	Terminal function name	Explanation
1	PB3/PP11	O	CMOS	Z	H - SW - P	VIDEO HEAD switching pulse output terminal
2	PB2/PP10	O	CMOS	Z	CAP ON	CAP motor ON/OFF control signal "H": Rotation ON
3	PB1/PP09	O	CMOS	Z	CAP FWD	Capstan rotation direction control signal "H": Forward rotation
4	PB0/PP08	O	CMOS	Z	AVD REC	Record: H
5	PC7/RT07	O	CMOS	Z	DCI SCS -	Serial transfer chip selection for DCI
6	PC6/RT06	O	CMOS	Z	SERVO REF30	Microprocessor internal servo reference 30 Hz signal
7	PC5/RT05	O	CMOS	Z	L/M FOR	OFF / Loading / UN - Loading / Branc
8	PC4/RT04	O	CMOS	Z	L/M REV	L/M FOR: L / H / L / H L/M REV: L / L / H / H
9	PC3/RT03	O	CMOS	Z	PB - L	
10	PC2/RP02	I	CMOS	Z	SW A	Mechanism position SW A
11	PC1/PP01	I	CMOS	Z	SW B	Mechanism position SW B
12	PC0/PP00	I	CMOS	Z	SW C	Mechanism position SW C
13	PJ7	O	CMOS	Z	DRM START	Drum start driver constant selection
14	PJ6	I	CMOS	Z	PROTECT SW	REC PROTECT detection
15	PJ5	I	CMOS	Z	SEP IN -	S terminal detection Detection:"L"
16	PJ4	I	CMOS	Z	SMMASK	Breakage detection input from transport
17	PJ3	I	CMOS	Z	PF	Pilot frame input
18	PJ2	O	CMOS	Z	LSI A/D	LSI parallel control Adr/Data selection
19	PJ1	O	CMOS	Z	RESETP	LSI RESET PC I/O RESET
20	PJ0	O	CMOS	Z	PACK	LP tape playback: H
21	PD7/HALT	O	CMOS	Z	DATA B7	(MSB)
22	PD6/BRQ	O	CMOS	Z	DATA B6	
23	PD5/BRK	O	CMOS	Z	DATA B5	
24	PD4/SYNC	O	CMOS	Z	DATA B4	Digital LSI parallel data (8 bit)
25	PD3/C	I	CMOS	Z	DATA B3	
26	PD2/R.W	I	CMOS	Z	DATA B2	
27	PD1/WR	I	CMOS	Z	DATA B1	
28	PD0/RD	I	CMOS	Z	DATA B0	(LSB)
29	PH7	O	Nch	Z	AUDIO PCS -	Parallel transfer chip selection for each LSI / AUDIO
30	PH6	O	Nch	Z	DCI PCS -	/ DCI
31	PH5	O	Nch	Z	DIF_READY	(SEL 135CLK)
32	PH4	O	Nch	Z	LSI W/R -	/ WRITE/READ
33	PH3	O	Nch	Z	LSI LT	Parallel transfer communication control for each LSI / ADR/DATA -
34	PH2	O	Nch	Zrre	E²PROM MCS	Mechanism E²PROM chip selection signal
35	PH1	O	Nch	Z	ST SNC LED	Start Sensor detection LED output "L": Drive
36	PH0	O	Nch	Z	END SNS LED	End detection LED output "L": Drive
37	MP	I	Nch		MP	Microprocessor mode selection "L" = GND
38	RST-	I			RESET	Reset input "L": Active
39	Vss				GND	

No.	Terminal name	I/O	Type	*1	Terminal function name	Explanation
40	X'tal	O			X'tal	Crystal connection terminal for system clock oscillation 12 MHz: Oscillation
41	EXTAL	I			EXTAL	
42	CS0 -	I		Z	READY IN	System controller serial communication READY
43	SIO	I		Z	SLV DATA	Serial data input from system controller
44	SO0	O		Z	SYS DATA	Serial data output to system controller
45	SCK0 -	I/O		Z	SLV CLK -	System controller serial communication CLOCK
46	BF7/AN11	O	CMOS	Z	E²PROM CLK	Clock to E²PROM
47	PF6/AN10	O	CMOS	Z	E²PROM DO	Output data to E²PROM
48	PF5/AN9	O	CMOS	Z	PB H	RF system mode selection: REC - P / REC / PB / After recording REC H: L / H / L / H PB H: L / L / H / H
49	PF4/AN8	O	CMOS	Z	REC H	
50	AVss				GND	A/D converter GND terminal
51	AVref				SYS 3V	A/D converter reference voltage input terminal
52	AVdd				SYS 3V	A/D converter positive power supply terminal
53	PF3/AN7	I	Hi - z	Z	E²PROM DI	E²PROM serial input data
54	PF2/AN6	I	Hi - z	Z	TAP2	Tracking position 2
55	PF1/AN5	I	Hi - z	Z	TAP1	Tracking position 1
56	PF0/AN4	I	Hi - z	Z	ATF TEMP	Tracking position 0
57	AN3	I	Hi - z	Z	TAPE SENS	Tape S/E sensor Detection voltage input A/Dinput terminal
58	AN2	I	Hi - z	Z	TEMP	Temperature input
59	AN1	I	Hi - z	Z	PB ENV	Playback envelope detection input A/Dinput terminal
60	AN0	I	Hi - z	Z	ATF ERROR	ATF ERROR (ATF LOCK error) input A/Dinput terminal
61	PG7/EXI1	I	Hi - z	Z	TUP REEL	TAKE UP REEL pulse input A/Dinput terminal
62	PG6/EXI0	I	Hi - z	Z	SUP REEL	SUPPLY REEL pulse input A/Dinput terminal
63	PG5/SYNC	I	Hi - z	Z	TRP 3	Tracking position 3
64	PG4/SYNC	I	Hi - z	Z	REF30	Reference timing signal from FP_S LSI
65	PG3/PBCT	I	Hi - z	Z	H_ADJ	ITI END detection pulse (for SWP adjustment)
66	PG2/DPG	I	Hi - z	Z	DRUM PG IN	DRUM PG input FRC capture input terminal
67	PG1/DFG	I	Hi - z	Z	DRUM FG IN	DRUM PG input FRC capture input terminal
68	PG0/CFG	I	Hi - z	Z	CAP PG IN	CAPSTAN FG FRC capture input terminal
69	PE7/DAB1	O	CMOS	H	CAP CTL	(NC)
70	PE6/DAB0	O	CMOS	H	LSI RESET	Reset for all LS
71	PE5/DAA1	O	CMOS	Z	DRUM ON	DRUM drive control signal "H": ON
72	PE4/DAA0	O	CMOS	Z	DRUM D/A	DA gate pulse output for DRUM ERROR output
73	PE3/PWM1	O	CMOS	Z	CAP PWN	PWM output terminal for CAP ERROR output
74	PE2/PWM0	O	CMOS	Z	CKGEN RST	Clock generator RESET
75	PE1/EC -	I	Hi - z	Z	CAP FG	CAP FG input terminal for TAPE COUNTER drive
76	PE0/INTO	O	CMOS	Z	HIDER	
77	PI7/SI1	I	Hi - z	Z	LSI SI	Serial input data from each LSI
78	PI6/S01	O	CMOS	Z	LSI SO	Serial output data to each LSI
79	PI5/SCK1	O	CMOS	Z	LSI CK	Serial clock output to each LSI
80	PI4/INT1	O	CMOS	Z	ERROR - H	
81	PI3/TO/D	O	CMOS	Z	FRMEND	
82	PI2/PWM	O	CMOS	Z	TIA DET	

No.	Terminal name	I/O	Type	*1	Terminal function name	Explanation
83	PI1/RMC	O	CMOS	Z	TRP - 0	Tracking position 3
84	TEX	I			NC	
85	TX	O			NC	
86	Vss				GND	GND terminal
87	Vdd				SYS 3V	Positive power supply terminal
88	NC				SYS 3V	(To be connected to Vdd)
89	PA7/PP07	O	COMS	Z	AUDIO SCS -	AUDIO serial transfer chip selection
90	PA6/PP06	O	COMS	Z	CODEC SCS -	CODEC serial transfer chip selection
91	PA5/PP05	O	COMS	Z	PPC SCS -	PPC serial transfer chip selection
92	PA4/PP04	O	COMS	Z	PTW SCS -	PTW serial transfer chip selection
93	PA3/PP03	O	COMS	Z	SP/LP	
94	PA2/PP02	O	COMS	Z	W MASK H	CODEC WRITE MASK
95	PA1/PP01	O	COMS	Z	SLOW3	
96	PA0/PP00	O	COMS	Z	VECC SCS -	VECC serial transfer chip selection
97	PA7/PP15	O	COMS	Z	CHARGE ON	PLL free running control
98	PA6/PP14	O	COMS	Z	HSW HOLD	HSW HOLD pulse
99	PA5/PP13	O	COMS	Z	SLOW 2	
100	PA4/PP12	O	COMS	Z	SLOW 1	

1394 microprocessor (100VQFP 0.5mm pitch)

*1 State of port in case of microprocessor resetting

No.	Terminal name	I/O	Type	*1	Terminal function name	Explanation
1	PB3/PP11	O	CMOS	Z	LINK_RESET	
2	PB2/PP10	O	CMOS	Z	DROP_FP	
3	PB1/PP09	O	CMOS	Z	CONST_RST	
4	PB0/PP08	O	CMOS	Z	FP_MASK	
5	PC7/RT07	O	CMOS	Z	PBUS7	
6	PC6/RT06	O	CMOS	Z	PBUS6	
7	PC5/RT05	O	CMOS	Z	PBUS5	
8	PC4/RT04	O	CMOS	Z	PBUS4	
9	PC3/RT03	O	CMOS	Z	PBUS3	
10	PC2/PP02	I	CMOS	Z	PBUS2	
11	PC1/PP01	I	CMOS	Z	PBUS1	
12	PC0/PP00	I	CMOS	Z	PBUS0	
13	PJ7	O	CMOS	Z	AD15	
14	PJ6	I	CMOS	Z	AD14	
15	PJ5	I	CMOS	Z	AD13	
16	PJ4	I	CMOS	Z	AD12	
17	PJ3	I	CMOS	Z	AD11	
18	PJ2	O	CMOS	Z	AD10	
19	PJ1	O	CMOS	Z	AD9	
20	PJ0	O	CMOS	Z	AD8	
21	PD7/HALT	O	CMOS	Z	AD7	
22	PD6/BRQ	O	CMOS	Z	AD6	
23	PD5/BRK	O	CMOS	Z	AD5	

No.	Terminal name	I/O	Type	*1	Terminal function name	Explanation
24	PD4/SYNC	O	CMOS	Z	AD4	
25	PD3/C	I	CMOS	Z	AD3	
26	PD2/R. W	I	CMOS	Z	AD2	
27	PD1/WR	I	CMOS	Z	AD1	
28	PD0/RD	I	CMOS	Z	AD0	
29	PH7	O	Nch	Z	NC	
30	PH6	O	Nch	Z	NC	
31	PH5	O	Nch	Z	NC	
32	PH4	O	Nch	Z	A5	
33	PH3	O	Nch	Z	A4	
34	PH2	O	Nch	Z	A3	
35	PH1	O	Nch	Z	A2	
36	PH0	O	Nch	Z	A1	
37	MP	I	Nch		MP	Microprocessor mode selection "L": GND
38	RST -	I			RESET	Resetting input "L": Active
39	Vss				GND	
40	X'tal	O			X'tal	Crystal connection terminal for system clock oscillation 12 MHz: Oscillation
41	EXTAL	I			EXTAL	
42	CS0 -	I		Z	DIF_READY	
43	SI0	I		Z	MEC_TO_DIF	
44	S00	O		Z	DIF_TO_MEC	
45	SCK0 -	I/O		Z	SCK	
46	PF7/AN11	O	CMOS	Z	NC	
47	PF6/AN10	O	CMOS	Z	MIC - ON	
48	PF5/AN9	O	CMOS	Z	MIC - 2	
49	PF4/AN8	O	CMOS	Z	MIC - 3	PB H L L H H
50	AVss				GND	A/D converter GND terminal
51	AVref				SYS 3V	A/D converter reference voltage input terminal
52	AVdd				SYS 3V	A/D converter positive power supply terminal
53	PF3/AN7	I	Hi - z	Z	AN7	
54	PF2/AN6	I	Hi - z	Z	AN6	
55	PF1/AN5	I	Hi - z	Z	AN5	
56	PF0/AN4	I	Hi - z	Z	AN4	
57	AN3	I	Hi - z	Z	DET_1394	
58	AN2	I	Hi - z	Z	MIC - 3	
59	AN1	I	Hi - z	Z	MIC - 2	
60	AN0	I	Hi - z	Z	MIC - 1	
61	PG7/EX11	I	Hi - z	Z	FPI1394	
62	PG6/EX10	I	Hi - z	Z	LCOM_FP	
63	PG5/SYNC	I	Hi - z	Z	PULL_UP	
64	PG4/SYNC	I	Hi - z	Z	FP	
65	PG3/PBCT	I	Hi - z	Z	INT	
66	PG2/DPG	I	Hi - z	Z	PACK	
67	PG1/DFG	I	Hi - z	Z	PULL_UP	

No.	Terminal name	I/O	Type	*1	Terminal function name	Explanation
68	PG0/CFG	I	Hi - z	Z	NC	
69	PE7/DAB1	O	CMOS	H	A -CS	
70	PE6/DAB0	O	CMOS	H	TP - S	
71	PE5/DAA1	O	CMOS	Z	PWR	
72	PE4/DAA0	O	CMOS	Z	PAD	
73	PE3/PWM1	O	CMOS	Z	PCLK	
74	PE2/PWM0	O	CMOS	Z	PLL_BIAS	
75	PE1 /EC -	I	Hi - z	Z	NC	
76	PE0/INTO	O	CMOS	Z	PULL_LP	
77	P17/SI1	I	Hi - z	Z	SYS_TO_DIF	
78	P16/S01	O	CMOS	Z	DIF_TO_SYS	
79	P15/SCK1	O	CMOS	Z	DIF_CLK	
80	P14/INT1	O	CMOS	Z	NC	
81	P13/TO/D	O	CMOS	Z	NC	
82	P12/PWM	O	CMOS	Z	NC	
83	P11/RMC	O	CMOS	Z	NC	
84	TEX	I			NC	
85	TX	O			NC	
86	Vss				GND	GND terminal
87	Vdd				SYS 3V	Positive power supply terminal
88	NC				SYS 3V	(To be connected to Vdd)
89	PA7/PP07	O	CMOS	Z	AUDIO SCS -	
90	PA6/PP06	O	CMOS	Z	CODEC SCS -	
91	PA5/PP05	O	CMOS	Z	PPC SCS -	
92	PA4/PP04	O	CMOS	Z	PTW SCS -	
93	PA3/PP03	O	CMOS	Z	WR	
94	PA2/PP02	O	CMOS	Z	IDIR	
95	PA1/PP01	O	CMOS	Z	RD	
96	PA0/PP00	O	CMOS	Z	NC	
97	PB7/PP15	O	CMOS	Z	NC	
98	PB6/PP14	O	CMOS	Z	NC	
99	PB5/PP13	O	CMOS	Z	PLL_SW2	
100	PB4/PP12	O	CMOS	Z	PLL_SW1	

IC704 E²PROM writing data.

IC701 system control Micon with build-in page 40 ~ 44.
Then VL - DC3S/H/E have to write into the next data for IC 704 E²PROM.

Address		
64	33	(Data of IC : 25 refer P44)
65	33	(Data of IC : 25 refer P44)

5. DC3 E²PROM CONTROL

E²PROM data setting content (system controller)

Addr	Name (corresponding RAM)	Description			Type
00	SYS _ROM _Ver	System controller ROM version No.			System code
01	kishu	(Main) Model selection code (Corresponding to product) *A"00):DH4000			
02	country	(Main) Destination selection code (Corresponding to designation) *B "00": Japan			
03	feature	(Main) Specification selection code (Corresponding to OEM) *C "00": Original			
04	meenu_sel	(Main) Menu selection code (Corresponding to OEM) *D "00": Original			
05	debug_sw	(Main) Software selection code (Corresponding to debug) *E "00h": Initial value			
06	bat_ref	(Main) Battery shut-down voltage adjustmentInitial value in nonset state = "85h"			
07	calendar	(Main) Initial year of data settingInitial value in nonset sate = "96h"			
08					
09	kishu _inv	(Aux) Addr "01" data content bit-inverted data			
0A	country_inv	(Aux) Addr "02" data content bit-inverted data			
0B	feature_inv	(Aux) Addr "03" data content bit-inverted data			
0C	menu _sel_inv	(Aux) Addr "04" data content bit-inverted data			
0D	debug_sw_inv	(Aux) Addr "05" data content bit-inverted data			
0E	bat_ref_inv	(Aux) Addr "06" data content bit-inverted data			
0F	calendar_inv	(Aux) Addr "07" data content bit-inverted data			
10	bl_ctl_adj[0]	Backlight light adjustment voltage change data	Forced max output	F1h V	Corresp-onding to change of setting
11	bl_ctl_adj[1]		LIGHT mode output	CAh V	
12	bl_ctl_adj[2]		Normal mode output	A4h V	
13	lamp_det_adj[0]	Lamp service life detection voltage change data	Min voltage	20h 0.90V	
14	lamp_det_adj[1]		Max voltage	57h 2.30V	
15	eep_lcd_v1 (V1)	Temperature detection judgment voltage Set conditions:V4>V3>V2>V1 n = Measurement data n<V1 is abnormal	V1≤ n<V2 0℃ or below	08h 0.1V	
16	eep_lcd_v2 (V2)		V2≤ n<V3 0℃ or – 10℃	056h 1.0V	
17	eep_lcd_v3 (V3)		V3≤ n<V4 10℃ or – 20℃	77h 1.6V	
18	eep_lcd_v4 (V4)		V4≤ n 20℃ or above Other judgment 50℃ or above	A3 2.1V 0C0h 2.3V	
19	eep_lcd_t1 (T1)	Lamp start voltage holding time Corresponding to forced max time change Set conditions: T1>T2>T3>T4	T1 0℃ or below / 4sec.	1E 120sec.	
1A	eep_lcd_t2 (T2)		T2 0 ℃ or – 10℃	0F 60sec.	
1B	eep_lcd_t3 (T3)		T3 10℃ or – 20℃	01A 40sec.	
1C	eep_lcd_t4 (T4)		T4 20℃ or above	00 0sec.	
1D	dew_ref[0]	Dew detection voltage change data (Detection>Cancel setting: Detection OFF	Cancel voltage	0Dh 0.8V	
1E	dew_ref[1]		Detection voltage	0Dh 0.8V	
1F	trk_adj_mode	1/4 track shift mode operation change data *F ("14": Initial value)			

Notes:

- Addr 01-07 data are read to judge only in resetting mode.
- In "FF" sate Addr 10-2F data judged to be unadjusted, and previously set initial value is adopted.
  (Aux) data is (Main) data bit-inverted data. Accordingly (Main) and (Aux) data are EXOR-ed in read mode.
  If "FF" is not obtained, the data must be ignored. In this case the initial value of bat_ref, calendar must be set on RAM.
- Output to D/A must be started and completed during picture muting after start-up of PCON.
- For *B to *F refer to the code table.

* ···If data is "00" at 20℃ or above the forced MAX is discontinued.

Addr	Name (corresponding RAM)	Description	PTC mode	Operation mode	Input/ output	Initial	Related D/A
20	da _cam15V	CAM-15V adjustment	–	CAM	OUT	80h	DA-A08
21	da clkgen pll	CLKGEN PLL adjustment		VCR STOP			
22	da_pco_y	PCO video output level ADJ	External sync 100% white		IN *2*3	81h	DA-A03
23	da_pco_c	Internal sync	Inner Sync Chroma blue		OUT *2*3	38h	DA-A04
24	da_v_agc	Y-EE level adjustment	External sync		IN *2*3	00h	DA-A28
25	da_alf_f1	ATF F1 frequency adjustment		PB *4	OUT *2	9ah	DA-A17
26	da_afl_f2	ATF F2 frequency adjustment				b1h	DA-A18
27	da_eq_trans_me	EQ transversal adjustment (ME)				92h	DA-A21
28	da_pll_shresh2	PLL thresh level 2 adjustment				6bh	DA-A20
29	da_dac_c					74h	DA-A11
2a	da_pll_freerun	PLL free run ADJ adjustment		PB*4*5		7fh	DA-A24
2b	da_pll_offset_me	PLL offset ADJ adjustment (ME)		PB*4		bah	DA-A25
2c	da_pll_frrn_tst	PLL free run ADJ adjustment test		PB*4*7	OUT *2	80h	DA-A24
2d	da_charge	Fade-out ALC charge discharge time, unit 45 ms		42h× 45ms = 3.0 sec.		42h	
2e	da_pll_offset_mp	PLL offset ADJ adjustment (MP)		PB*4	OUT *2	bah	DA-A25
2f	da_eq_trans_mp	EQ transversal adjustment (MP)				92h	DA-A21
30	da_rw_bcll	LCD R white balance adjustment		*6	IN	85h	DA-A12
31	da_bwb_cll	B white balance adjustment				75h	DA-A13
32	da_vco_adj	VCO adjustment				80h	DA-A26
33	da_com_bias	Common bial adjustment				73h	DA-A10

*1 CAM-L = "L" *2 AV - H = "H" *3 AV SEL = "H"
*4 Track judgment OFF *5 CHARGE ON signal: "H"
*6 VCR stop mode, backlight is forcible set to NORMAL.
*7 CHARG ON SIGNAL: L PLL free run is changed for test. Value of 2A is restored after the adjustment mode is canceled.

34	bat_meter_4	Battery remaining capacity indication Corresponding to thresh change	4/5 indication judgment voltage	87h	
35	bat_meter_3		3/5 indication judgment voltage	83h	
36	bat_meter_2		2/5 indication judgment voltage	80h	
37	bat_meter_1		1/5 indication judgment voltage	7bh	
38	eep_lamp_step	Backlight light reduction control Change of light reduction curve after forced acceleration	Time per 3 steps cut 0.5 sec	03h	
39	direct_adr	Corresponding to direct address change		40h	
3a	da_vol_ctl	User VR sound volume adjustment		ffh	
3b					
3c					
3d	da_dac_r			80h	DA-A14
3e	da_dac_g			80h	DA-A15
3f	da_dac_b			80h	DA-A16

6. LCD-DSP Adjustment data storage range

VCR ADJ	LCD bus	Function register name	Data bit	Description	Initial Value	RT
40	02	INSW DLATCH *	5 1 2	insw <4> <3> <2> <1> <0> dlaich ** '1' Clcv C to Ylcv Pcdestal Y-16 ⬆ down signed down comp on '0' thru hru thru thru Y-70 ⬇	F d8	○
41	03 04	PICORG Picture quality adjustment	8	picorg <7> <6> <5> <4> <3> <2> <1> <0> ± 1 1/2 1/4 1/8 1/16 1/32 1/64 Addition/subtraction level (complement of 2)	30	○
42	08	CNTORG Luminance adjustment	8	cntorg <7> <6> <5> <4> <3> <2> <1> <0> 1 1/2 1/4 1/8 1/16 1/32 1/64 1/128	80	○
43	0B	DPSW MATCSW CRBSW * HRT3 * HRTO	1 1 1 1 1 2 1	dpsw matcsw crbsw * hrt3 ** hrt0 '1' on Y/C Y/C H reset test5 '0' off DVTR DVTR Free run Normal	00	○
44		* HCMOD	6 2	* * * * * * hcmod <1> <0> "00" H:910 (Y/C NTSC) "01" H:908 (Y/C PAL) "10" H:858 (DVTR NTSC) "11" H:864 (DVTR PAL)	02	○
45	17	GPL peak adjustment	8	gpl <7> <6> <5> <4> <3> <2> <1> <0>	96	○
46	19	PEDESTAL Pedestal adjustment	8	pedestal <7> <6> <5> <4> <3> <2> <1> <0> The pedestal position is adjusted within -128 to +127 (common to RGB). Complement of 2 (Operation at wbmod = '0')	3D	○
47	20	TESTSW YCTEST0 YETEST1	2 3 3	testsw<1><0> yctest0<2><1><0> yctest1<2> <1> <0> "00" yctest0 "000" yp out "000" γ RAM R out "01" yctest1 "001" 1HRAM out "001" γ RAM G out "10" osdtest "010" B-Y out "010" γ RAM B out "11" ctltes "011" R-Y out "011" R out "100" MATRIX B out "100" G out "101" MATRIX G out "101" B out "110" MATRIX R out "110" COMMON out "111" APL out "111" ---	00	
48	21	DACOFF DOSW DLEVSW DTESTSW DCKSW	4 1 1 1 1	dacoff <3> <2> <1> <0> dosw levsw diestsw dcksw "1 ** * " R off '1' do output yin dlcv on ck inversion "*1* * " G off '0' Normal FF Normal Normal "**1 * " B off "*** 1 " COM off	00	○
49	40	DELTA VHSMSK DSM NTPA CLSINV SPSINV SP1 SP2	1 1 1 1 1 1 1 1	delta vhsmsk dsm ntpa clsinv spsinv sp1 sp2 '1' delta on dsm ntsc posi posi '0' stripe off Y/C pal nega nega	E2	○

VCR ADJ	LCD bus	Function register name	Data bit	Description	Initial Value	RT
4A	41	SWA CDSW MO1 MO2 EXINV1 EXINV2 HREVC VREVC	1 1 1 1 1 1 1 1	swa cdsw mo1 mo2 exinv1 exinv2 hrevc vrevc '1' off on in nin off off '0' on off nv nv rev rev	E7	○
4B	42	OSDSW CSPINV FRPCINV CTRINV LOWOINV GPSINV FRPVINV HQDATA<2>	1 1 1 1 1 1 1 1	osdsw csp rpc ctr lowo gps frpv hqdata <2> '1' nck HL~ posi posi WR posi posi '0' pck LH~ nega nega HO nega nega	F6	○
4C	43	HQDATA <10>~<3>	8	hqdata <10> <9> <8> <7> <6> <5> <4> <3>	99	○
4D	44	FRPCDATA <8>~<1>	8	frpcdata <8> <7> <6> <5> <4> <3> <2> <1>	2A	○
4E	45	CTRDATA <8>~<1>	8	ctrdata <8> <7> <6> <5> <4> <3> <2> <1>	3E	○
4F	46	SPDSAM SPDLY <7>~<1>	1 7	spdsam spddata <7> <6> <5> <4> <3> <2> <1> '1' H/L (pieces) '0' H (the same)	C6	○
50	47	WTVMASK SPDDLY<7>~<1> (CAM)	1 7	wivmask spddly <7> <6> <5> <4> <3> <2> <1> '1' ON '0' OFF'0'	18	○
51	48	SPDINV SPDSW WSPD<6>~<1>	1 1 6	spdinv spdsw wspd <6> <5> <4> <3> <2> <1> '1' posi posi '0' nega nega	AC	○
52	4A	NQLOAD WQLOAD CLSDATA<6>~<1>	1 1 6	nqload wqload clsdata <6> <5> <4> <3> <2> <1>	F2	○
53	4B	TESTCK VQLOAD FIEP OSDST OUTSW FOSC FRPSTOP OSPSTOP	1 1 1 1 1 1 1 1	testck vqload fiep osdst outsw fosc frpstop cspstop '1' vck off off nor off off off off '0' hck load rev test on adj stop stop	FF	○
54	02	INSW DLATCH(VCR) *	5 1 2	insw <4> <3> <2> <1> <0> dlaich * * '1' Clev C to Ylev Pedestal Y-16 ⬆ down signed down comp on '0' thru thru thru thru Y-70 ⬇	F8	○
55	03	PICORG Picture quality adjustment (VCR)	8	picorg <7> <6> <5> <4> <3> <2> <1> <0> ± 1 1/2 1/4 1/8 1/16 1/32 1/64 Addition/subtraction level (complement of 2)	30	○
56	04	CNTORG Luminance adjustment	8	cntorg <7> <6> <5> <4> <3> <2> <1> <0> 1 1/2 1/4 1/8 1/16 1/32 1/64 1/128	80	○
57	12	GRYLEV Gray output	8	grylev <7> <6> <5> <4> <3> <2> <1> <0> '1' Gray output Setting of 1/2 of indication level '0' normaly	40	○

VCR ADJ	LCD bus	Function register name	Data bit	Description	Initial Value	RT
58	47	WTVMASK SPDDLY<7>~<1> (VCR)	1 7	wtvmask spddly <7> <6> <5> <4> <3> <2> <1> '1' ON '0' OFF	20	○
59	0F	Color Level Mode change (CAM)	1 7	omixse bgorg <6> <5> <4> <3> <2> <1> <0> '1'Judgment is performed 1 1/2 1/4 1/8 1/16 1/32 1/64 '0'Judgment is not performed	40	—
5A	0F	Color Level Mode change (VCR)	1 7	omixse bgorg <6> <5> <4> <3> <2> <1> <0> '1'Individual operation 1 1/2 1/4 1/8 1/16 1/32 1/64 '0'bgain interlocking	40	—
5B	10	Color Level Mode change (CAM)	8	ggain <7> <6> <5> <4> <3> <2> <1> <0> '1'Individual operation 1 1/2 1/4 1/8 1/16 1/32 1/64 '0' bgain interlocking	40	—
5C	10	Color Level Mode change (VCR)	8	ggain <7> <6> <5> <4> <3> <2> <1> <0> '1'Individual operation 1 1/2 1/4 1/8 1/16 1/32 1/64 '0' bgain interlocking	40	—
5D	11	Color Level Mode change (CAM)	8	rgein <7> <6> <5> <4> <3> <2> <1> <0> '1'Individual operation 1 1/2 1/4 1/8 1/16 1/32 1/64 0' bgain interlocking	40	—
5E	11	Color Level Mode change (VCR)	8	rgein <7> <6> <5> <4> <3> <2> <1> <0> '1'Individual operation 1 1/2 1/4 1/8 1/16 1/32 1/64 0' bgain interlocking	40	—
5F	B3	OSD indication position	–	(VCR ADJ:5F) □□□□□□□□	98	—
60	B3	OSD indication position	–	Command (B3h) (VCR ADJ:60) ■■■■■■■□□□□□□□ □□□□□□□□ Y start position	15	—
61	B3	OSD indication position	–	(VCR ADJ:61) □□□□□□□□ □□□□□□□□ X start position	07	—
62	B3	OSD indication position	–	d'ont care (VCR ADJ:62) □□□□□□□□ □□□□□□□□ Y end position	00	—
63	B3	OSD indication position	–	(VCR ADJ:63) □□□□□□□□ □□□□□□□□ X end position	E7	—
64	B4	DOT delay value	–	Command (B4h) (VCR ADJ:64) ■■■■■■■□□□□□□□□ RED delay	22	—
65	B4	DOT delay value	–		22	—
66	B4	DOT delay value	–	(VCR ADJ:65) □□□□□□□□□ GREEN delay (VCR ADJ:66) □□□□□□□□□ BLUE delay d'ont care	22	—
67	–	BRTA0	–	BRTA value at USER BRIGHT center	32	—
68	–	BRTB γ	–	BRTB value at intersection with γ 0	2D	—
69	–	COMLEV0	–	COMLEV value at intersection with γ 0	58	○
6A	–	x0	–	R-Y axis correction	7B	—
6B	–	R-Y axis correction	–	Center value of ROM table input amplitude	80	○
6C	–	Color level change width	–	USER VR COLOR change width	64	—
6D	–	USER VR BRIGHT	–	Brightness adjustment	80	○
6E	–	USER VR COLOR	–	Color density adjustment	80	○
6F	–	USER VR TINT	–	Color hue adjustment	80	○

70	ZOOM_thresh[0]	Zoom ASW judgment threshold value	(TELE)360-180 pps	033h .V	Corre-sponding to change of setting
71	ZOOM_thresh[1]		(TELE)180-120 pps	048h .V	
72	ZOOM_thresh[2]		(TELE)120- 60 pps	05ch .V	
73	ZOOM_thresh[3]		60- OFF	071h .V	
74	ZOOM_thresh[4]		FF- 60 pps	08fh .V	
75	ZOOM_thresh[5]		(WIDE) 60-120 pps	0a4h .V	
76	ZOOM_thresh[6]		(WIDE)120-180 pps	0b8h .V	
77	ZOOM_thresh[7]		(WIDE)180-360 pps	0cdh .V	

78	Pll_offset_corr	PLL OFFSET High-order 4-bit : correction value of 62℃or above Temperature compensation correcting value Low-order 4-bit : correction value of 48℃ or above but lower than 62℃	42h	
79	Frame posi	Frame in case of multimedia photographing	3Ch	
7a				

Area to be used on automatic machine (8 byte)

7B		Other uses are prohibited since the item is used as work on the automatic machine.	
7C			
7D			
7E			
7F			

7. Data storage area for mechanism (mechanism controller)

Addr	Name (corresponding RAM)	Description		Type
100	Mechanism change No.	Mechanism design change No.		System Code
101				
102				
103				
104	HSWP ADJ	HSWP adjustment data		
105	da_rec	REC level (record current) *8	60h	DA1-A19
106	ffrew_dir	CAP direction in case of FFREW (m_mech is given)		
107	mcc_time [0]	Year, month An example: March, 1995 ➡53h		Mechanism code
108	mcc_time [1]	Day 20 ➡20h		
109	mcc_time [2]	Hour 14 ➡14h		
10A	mcc_time [3]	Minute 59 min ➡59h		
10B	mcc_time [4]	Second 59 sec ➡59h		
10C	se sense	S/E sensor detection level change data		
10D	tape_rcf	Tape sensor detection voltage change data	03Fh(1.2V)	
10E	clog_rcf	Clogging judgment voltage change data	0B9h(1.35V)	
10F	corr_3db	Playback interchange judgment level change data	046h 50%(PCM) 60%(Nor)	
110	OPETIME_1(0) LSB	Drum motor operation time total Unit: Sec 0-FFFFFF: Max 16,770,000 seconds = Approx. 4,660 hrs)	00%	
111	OPETIME_1(1)		35%	
112	OPETIME_1(2) MSB		40%	
113	OPETIME_2(0) LSB	Capstan motor operation time total Unit: Sec 0-FFFFFF: Max 16,770,000 seconds = Approx. 4,660 hrs)	45%	
114	OPETIME_2(1)		50%	
115	OPETIME_2(2) MSB		55%	
116	OPETIME_3(1) L	Number of cassette ejections Unit: Times (Max 65,535 times)	60%	
117	OPETIME_3(1) H		65%	
118			70%	
119			75%	
11A	CLOG_TIMES(0) L	Clogging detection number Unit: Times (Max 65,535 times)	80%	
11B	CLOG_TIMES(1) H		85%	
11C	DEW_TIMES(0) L	Dew alarm number Unit: Times (Max 65,535 times)	90%	
11D	DEW_TIMES(1) H		95%	
11E			100%	
11F				
120-125	PBRF_ENV_FWD	Playback RF envelope measurement point data (Track shifting FWD direction)		
126-12B	PBRF_ENV_REW	Playback RF envelope measurement point data (Track shifting REW direction)		

*8 REC-H: "H", REC GATE:"H", HSWP:"H"

Addr	Name (corresponding RAM)	Description				Type
12C	MEC_ERROR(0)	Status(current)upon occurrence of mechanism error (ErrorNo.,operation state of mechanism, servo and system *G)			Exxx	
12D	MEC_ERROR(1)				m_smod	
12E	MEC_ERROR(2)				vcr mode	
12F	MEC_ERROR(3)				m_system	
130	MEC_ERROR(4)	Status (justbefore) upon occurrence of mechanism error (ErrorNo., operation state of mechanism, servo and system *G)			Exxx	
131	MEC_ERROR(5)				m_smod	
132	MEC_ERROR(6)				vcr mode	
133	MEC_ERROR(7)				m_system	
134	servo func	Servo special function Ffh: All is invalid.			32h	*H
135	PPC STD TIMER	PPC STD TIMER (Unit 0.1 s)			ffh	
136	DCI SYNC SW	DCI serial communication content SW 1st byte bit 0-6			54h	
137	VMUTE LEVEL	Screen mute SYNC error level			12h	
138	VMUTE TIMER	VMUTE timer in case of PB in STOP state			ffh	
139	DCI PCOMP PB	DCI serial communication content (in case of ISP COMP PB)			ffh	
13A	DCI ISPCOMP VS	DCI Serial communication content (in case of ISP COMP search FF REWV)			ffh	
13B	DCI BITABI	DCI Serial communication content (23REG_LV, 45AD_LV, 6VTB_H)			ffh	
13C	CODEC1 MVDETTH	CODEC1 serial communication content (MVDET thresh)			ffh	
13D	CODEC1 SW	CODEC1 Serial communication content SW 1FILTER 234 RUD 5CKRST			ffh	
13E	PTC SW	PTC Serial communication content SW VCR 1st byte bit 0-6			ffh	
13F	AUDIO MUTE LVL	AUDIO serial communication content (MUTE LEVEL)			ffh	
140	Pb_gain_f	Capstan (SP)	Playback	Speed gain change data	Speed gain correction	0FFh	*I
141	pb_gain_p			Phase gain change data	Phase gain correction	0FFh	
142	asm_gain_f		ASM	Speed gain change data	Speed gain correction	0FFh	
143	asm_gain_p			Phase gain change data	Phase gain correction	0FFh	
144	iti_gain_f		ITI	Speed gain change data	Speed gain correction	0FFh	
145	iti_gain_p		ITI	Phase gain change data	Phase gain correction	0FFh	
146	vsf_gain_f		VSF	Speed gain change data	Speed gain correction	0FFh	
147	vsf_gain_p			Phase gain change data	Phase gain correction	0FFh	
148	vsr_gain_f		VSR	Speed gain change data	Speed gain correction	0FFh	
149	vsr_gain_p			Phase gain change data	Phase gain correction	0FFh	
14A	vsf_gain_f	Capstan (LP)	Playback	Speed gain change data	Speed gain correction	0FFh	
14B	vsf_gain_p			Phase gain change data	Phase gain correction	0FFh	
14C	vsr_gain_f		ASM	Speed gain change data	Speed gain correction	0FFh	
14D	vsr_gain_p			Phase gain change data	Phase gain correction	0FFh	
14E	vsf_gain_f		ITI	Speed gain change data	Speed gain correction	0FFh	
14F	vsf_gain_p			Phase gain change data	Phase gain correction	0FFh	
150	vsr_gain_f		VSF	Speed gain change data	Speed gain correction	0FFh	
151	vsr_gain_p			Phase gain change data	Phase gain correction	0FFh	
152	slow_gain_f		VSR	Speed gain change data	Speed gain correction	0FFh	
153	fr_gain_f			Phase gain change data	Phase gain correction	0FFh	
154	d_com_g_a		SLOW Speed gain change data		Speed gain correction	0FFh	
155	drm_gain_f		FF/REW Speed gain change data		Phase gain correction	0FFh	
156	drm_gain_p	Drum	Increasing speed gain change data			0FFh	
157			Speed gain change data		Speed gain correction	0FFh	
158			Phase gain change data		Phase gain correction	0FFh	

Addr	Name (corresponding RAM)	Description		Type
159	lsi_func	LSI function selection	ffh	*J
15A	lsi_func_sw2	LSI function selection 2	ffh	*K
15B	lsi_ck_3_mstr	LSI function selection 3	ffh	*L
15C	trackout_lvl	Drum phase deviation judgment level	e1h	
15D	w_mask_lvl	Screen updating prohibition level	40h	
15E	clog_offset	Envelope detection circuit offset (Automatic writing after running interchange CK)	00h	
15F	w_mask_ok_lvl	Screen updating prohibition cancel level	ffh	
160	w_mask_sync_th	w_mask control SYNC thresh level	94h(148d)	
161	track_sft_lvl	Track shift level in different mode	80h	
162	PTW SW1	PTW serial communication content SW 1st byte bit 6	ffh	
163	PTW SW2	PTW serial communication content SW 2nd byte bit 0-6	ffh	
164	VBLUE TIME	Number of frames until pull-muting after data is not fetched	0Ah	
165	d_clog_lvl	VECC error clogging judgment level	0Ah	
166	offset_adj_st	PLLoffset rough adjustment start position	b4h	
167	offset_1st_digit	Plloffset value	05h	
168	offset_2st_step	Number of Plloffset steps (total number of steps)	08h	
169	trans_adj_st	Plltrans rough adjustment start position	20h	
16A	trans_1st_digit	Plltrans value	08h	
16B	trans_2st_step	Number of PLLtrans steps (total number of steps)	08h	
16C	trans_center	PLLtrans (value during offser rough adjustment)	30h	
16D	pll_me_lvl	PLL ME adjustment NG level (/16)	0Ch	
16E	pll_mp_lvl	PLL MP adjustment NG level (/16)	0Ch	
16F	sync_err_lvl	Significant error judgment level in case of PLL adjustment	64h(100)	
170	pll rec timer	PLL REC time Unit: 0.5 sec	50h	
171	pll vsr timer	PLL VSR time Unit: 0.5 sec	06h	
172	pll pb timer	PLL PB time Unit: 0.5 sec	0Ah	
173	trk sft lvl	Track shift value in case of running interchange	0FFh	
174	corr result	Result of judgment in case of running interchange inspection	0FFh	
175	ffrew tape lmt	Tape end detection level in case of FFREW (66h: Near tape end)	090h	
176	PTW SW4	PTW serial communication content SW 4th byte bit 0-6	0FFh	
177	PTW SW5	PTW serial communication content SW 5th byte bit 0, 1	0FFh	
178	PTW SW14	PTW serial communication content SW 2nd byte bit 2, 3, 4	0FFh	

Addr	Name (corresponding RAM)	Description		Type
179	ffrew mask cnt	FFREW building-up mask count	014h	
17A	audio _mute_do	Mute generation timing in case of SPLP selection	003h	
17B	audio_mute_len	Mute time in case of SPLP selection	00Fh	
17C	pb hold lvl	Screen hold level in case of normal PB	040h	
17D	CAP OFF TIMER	CAP OFF timer in case of FFREW (unit 1.365 ms)	024h	
17E	CHIP ID 0	Chip ID	0FFh	
17F	CHIP ID 1	Chip ID		
180	CHIP ID2	Chip ID		FF
181	CHIP ID3	Chip ID		00
182	CHIP ID4	Chip ID		01
183	1394SW	7 Trouble CK, 6 5: ON EE OUT OFF, 5 VCRPB: OUT ON 4 Audio mute request is aborted in case of blanking., 3 mic data FF 2 1: ON recp DIFOFF, 1 dif camera ON , 0 chipID indication		
184	vspb mute	Mute time prolongation in case of PB from search state		
185	DIF TEST			
186	TX_OFFSET_L			
187	TX_OFFSET_H			
188	RX_OFFSET_L			
189	RX_OFFSET_H			
18A-191	CODEC_SET2-9	CODEC 2nd-9 byte		
192-199	CODEC_INI_SET2-9	CODEC 2nd-9 byte (table value change)		
19A	TRANSE SET ERR	TRANSPORT error FF or 0 a+b 1a 2b		
19B	DCI_SET1	DCI 1st byte change		
19C	DCI_SET10	DCI 10th byte change		
19D	DCI_SET13	DCI 13th byte change		
19E	DCI_SET11_pb	DCI PB 11th byte change		
19F	DCI_SET11_vs	DCI VS 11th byte change		
1A0	DCI_SET12_pb	DCI PB 12th byte change		
1A1	DCI_SET12_vs	DCI VS 12th byte change		
1A2	DCI_SET10_dif	DCI D 10th byte change		
1A3	DCI_SET10_nor	DCI N 10th byte change		
1A4	DCI_SET13_dif	DCI D 13th byte change		
1A5	DCI_SET13_nor	DCI N 13th byte change		
1A6	DCI_SET1_nor	DCI D 1st byte change		
1A7	DCI_SET1_dif	DCI N 1st byte change		
1A8	DCI_SET3_nor	DCI D 3rd byte change		
1A9	DCI_SET3_dif	DCI N 3rd byte change		
1AA	VS_DLY_CNT	Search mode prolongation time setting		
1AB	SC TIMING SET	Subcode read timing setting		
1AC-1FE SET		Mechanism controller ROM version No.		
1FF	meca con ver_no			

*A Details of model development codes (for categories)(01h)

Code	Setting description	Data setting							
		b7	b6	b5	b4	b3	b2	b1	b0
0	Original model (DH4000)	0	0	0	0	0	0	0	0
1	DC2	0	0	0	0	0	0	0	1

*B Details of destination codes (for specification change of each destination)

Destination / Specification item	Japan (U.C)	North America (S.H)	EC (E)	Southeast Asia
Destination code (hexadecimal)	00	01	0A	0B
NTSC/PAL	NTSC		PAL	
AV external storage unit	×	×	×	×
Clock display/setting	Year, Month, Day	Month, day, year	Day, month, year	Day, month, year
12-h/24-h system	AM/PM (0-11)12H	(1-12)12H AM/PM	24H (0-23)	24H (0-23)

*C Details of specification changeover codes (03h)

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications (in accordance with model code)	0	0	0	0	0	0	0	0
0	Abolishment of tuner connection	*	*	*	*	*	*	*	1
1	Addition of I/O contacts *1	*	*	*	*	*	*	1	*
2	Abolishment of wide screen changeover function	*	*	*	*	*	1	*	*
3	Fixing SP mode	*	*	*	*	1	*	*	*
4	Fixing LP mode	*	*	*	1	*	*	*	*
5	Turning ON of MIC data writing special function	*	*	1	*	*	*	*	*
6		*	1	*	*	*	*	*	*
7	Abolishment of still unit connection	1	*	*	*	*	*	*	*

*1 Addition of I/O contacts enables storage in AV external storage unit

***D Details of menu selection codes (04h)**

Code	Setting description	Data setting							
		b7	b6	b5	b4	b3	b2	b1	b0
	Original model	0	0	0	0	0	0	0	0
0-7		*	*	*	*	*	*	*	*

***E Details of menu selection codes (05h)**

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications	0	0	0	0	0	0	0	0
0	Increasing clock count speed to high (1 min. to 0.5 s.)	*	*	*	*	*	*	*	1
1		*	*	*	*	*	*	1	*
2	Increasing clock count speed to extremely high (1 day to 0.5 s.)	*	*	*	*	*	1	*	*
3	Increasing 60-minute dew to high (1 min. to 1.0 s.)	*	*	*	*	1	*	*	*
4		*	*	*	1	*	*	*	*
5	Aging mode (Play-REW-Play)	*	*	1	*	*	*	*	*
6	Elimination of still/slow mode time limit	*	1	*	*	*	*	*	*
7	Abolishment of FF/REW 60-time speed	1	*	*	*	*	*	*	*

***F Details of codes for 1/4-track shift operation change (for test mode and specification change)**

Serial No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
0	Original specifications (only 1/4-fast tracking)	0	0	0	0	0	0	0	0
1-7F	1/4-fast ⟷ Center ⟷ Slow	0	0	0	0	0	0	0	1
80	Original specifications (only 1/4-fast tracking)	1	0	0	0	0	0	0	0
81-FF	1/4-fast ⟷ Center ⟷ Slow	1	0	0	0	0	0	0	1

When the bit 7 is HI: Matsushita's spec.; Low, our own recording spec.

*G List of status codes for occurrence of mechanical errors(Ach-B3h)

Exxx	Setting description
07	CAP FG signal has not been entered for 1 s. or longer.
11	Although L/M has been turning in the forward direction for 5 s. or longer, it does not move to the next mechanical position.
12	Although L/M has been turning in the rearward direction for 5 s. or longer, it does not move to the next mechanical position.
20	For 6 s. after drum starts, speed lock has not been enabled or speed lock was once enabled but then has been disabled.
25	TU reel sensor is switched on.
26	RU reel sensor is switched on

Value	m_smod	vtrmode (7-4, 3-0) Servo mode	vtrmode (7-4, 3-0) CAP speed	m_system
00	Normally	EJECT	08	INIT
01	Loading to MP	STOP	00	EJECT
02	Loading from MP	FF	-	STOP
03	Unloading to MP	REW	-	FF
04	Unloading from MP	PB	81	REW
05	At drum start operation (At unloading)	STILL	01	PB
06		SLOW	01	STILL
07		VSF-8	08	SLOW
08	During action against mechanical error	VSR-4	04	Blank & pause
09		VSR-8	08	VSF
0A		VSR-6	06	VSR
0B		REC	01	REC
0C		ASM-1	01	REC PAUSE
0D		ASM-3	03	Recording search, forward
0E		CAMR-3	03	Recording search, rearward
0F		TURN-3	03	Recording search, still
10				HSWP automatic adjustment
11				Recording current adjustment
12				Feed compatibility inspection
FF	At mechanical initialization			

*H Setting of servo special functions (B4h)

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications	0	0	0	0	0	0	0	0
0	15-time speed at the FF/REW tape end	*	*	*	*	*	*	*	1
1	Starting FF/REW speed reduction earlier	*	*	*	*	*	*	1	*
2	Using brake with solenoid valve	*	*	*	*	*	1	*	*
3	Complying with DH4000 at FF/REW tape end	*	*	*	*	1	*	*	*
4	Fixing VCR mode to camera SPLP mode (When PAL is OFF, SP is fixed; ON, SPLP is automatically identified.)	*	*	*	1	*	*	*	*
5	Fixing LP mode	*	*	1	*	*	*	*	*
6	Turned on drum gain changeover	*	1	*	*	*	*	*	*
7	Turned on capstan gain changeover	1	*	*	*	*	*	*	*

*I Details of capstan, drum gain compensation

Setting cap_gain_sw (adr:CEh) to 01h compensates the capstan gain.
Setting drm_gain_sw (adr:CFh) to 01h compensates the drum gain.
Capstan gain **_gain_f: Compensates the speed system, speed integral system gain.
**_gain_p: Compensates the phase system, phase integral system gain.
Drum gain **_gain_f: Compensates the speed system, acceleration system gain.
**_gain_p: Compensates the phase system, phase integral system gain.
The compensation procedures are as follows.
When the gain on ROM is + 7 dB and the compensation value is -3dG (data of 03h):(+7 dB) + (-3 dB) = + 4dB
To make the gain minimum (null), write FEh.

Compensation Value dB	Data	Compensation Value dB	Data	Compensation Value dB	Data	Compensation Value dB	Data
12db	20h	06db	10h	00db	00h	-06db	18h
11db	21h	05db	11h	-01db	01h	-07db	19h
10db	22h	04db	12h	-02db	02h	-08db	1Ah
09db	23h	03db	13h	-03db	03h	-09db	1Bh
08db	24h	02db	14h	-04db	04h	-10db	1Ch
07db	25h	01db	15h	-05db	05h	-11db	1Dh

*J LSI special function setting 1 (159h)

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications	0	0	0	0	0	0	0	0
0	Set audio serial port for new LSI	*	*	*	*	*	*	*	1
1	Disabling the screen mute under the inhibit mode	*	*	*	*	*	*	1	*
2	Displaying each LSI error under the error display mode (note 1)	*	*	*	*	*	1	*	*
3	Displaying the track No. under the error display mode	*	*	*	*	1	*	*	*
4	Displaying the screen breakdown evaluation level under the error display mode	*	*	*	1	*	*	*	*
5	Disabling w_mask at screen breakdown.	*	*	1	*	*	*	*	*
6	Setting audio delay bit to 0.	*	1	*	*	*	*	*	*
7	Displaying the error display mode chip ID	1	*	*	*	*	*	*	*

Note 1: Displaying each LSI error under the error display mode.
Each LSI serial communication error; 15-count display; PTC, PCI, VECC, DCI, FAIL, CODEC, TRACKOUT, and AUDIO from left.

Note 2: Displaying the track No. under the error display mode.
The upper three bytes are assigned to the track No.; the least significant byte is assigned to ISP read data.
LSI special function setting 2 (15Ah)

Note 3: Displaying the screen breakdown evaluation level under the error display mode.
The most significant byte is assigned to No. of times of PTCRST;
the second most significant byte is assigned to specifying FF at w_mask;
the third and forth bytes are assigned to the w_mask evaluation function value.

*K LSI special function setting 2(15Ah)

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications	0	0	0	0	0	0	0	0
0	IActuating the search mode for a minor error and the w_mask mode for a major error (Note 1)	*	*	*	*	*	*	*	1
1	Fixing fp_fr_v to HI for vecc TS4	*	*	*	*	*	*	1	*
2	Communicating using audio ch2 during recording	*	*	*	*	*	1	*	*
3	Eliminating mechanical errors	*	*	*	*	1	*	*	*
4	Not using FRDET for SPLP changeover	*	*	*	1	*	*	*	*
5	Using rec invalid	*	*	1	*	*	*	*	*
6	Disabling automatic REC during PLL AUTO ADJ	*	1	*	*	*	*	*	*
7	Interlock still unit with CAP off	1	*	*	*	*	*	*	*

Note 1: As a rule, the search is not executed for a minor error.
During operation, be sure to set the LSI special function setting bit 5 to OFF.
For the search mode, use a value 16 times the screen update disabling canceling value.
For w_mask mode, use the screen update disabling value.

*L LSI special function setting 3 (15Bh)

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications	0	0	0	0	0	0	0	0
0	VBID ON	*	*	*	*	*	*	*	1
1	Fixing PLL adjustment to SP	*	*	*	*	*	*	1	*
2	Fixing only mechanical controller to PAL	*	*	*	*	*	1	*	*
3	Disabling PPC separate mode (*1)	*	*	*	*	1	*	*	*
4	Using ITI servo for LP	*	*	*	1	*	*	*	*
5	DRM_NOWAIT	*	*	1	*	*	*	*	*
6	Inverting the polarity of HSWPHOLD at PB	*	1	*	*	*	*	*	*
7	Using ITI servo for SP	1	*	*	*	*	*	*	*

*1 Inverting polarity from V17

***L 1394 special function setting 3 (183h)**

Bit No.	Setting description	Data setting							
		b7	b6	b5	b4	b3	bb2	b1	b0
	Original specifications	0	0	0	0	0	0	0	0
0	I Getting the chip ID (The display is set at 159.)	*	*	*	*	*	*	*	1
1	Setting DIF to ON under the CAM mode.	*	*	*	*	*	*	1	*
2	When DIF is set to ON under the CAM mode,setting DIF to OFF at RECP.	*	*	*	*	*	1	*	*
3	Fixing MIC data to FFh.	*	*	*	*	1	*	*	*
4	Abolishing the analog muting at a blank.	*	*	*	1	*	*	*	*
5	Setting OUT to ON at VCRPB.	*	*	1	*	*	*	*	*
6	When the bit 5 is set to ON, setting OUT to OFF at EE.	*	1	*	*	*	*	*	*
7	For check of correction regarding whether tape is detected.	1	*	*	*	*	*	*	*

8. E²PROM ADDRESS MAP

ADRS	PART	LABEL		DSP ADRS	Description		MAX	NTSC	PAL
000	CAM DSP	WB_INDOR_R_W	(H)	5A	White balance adjustment value R(3200K)	*	03	00	00
001	CAM DSP		(L)	5B			FF	09	90
002	CAM DSP	WB_INDOR_B_W	(H)	5C	White balance adjustment value B(3200K)	*	03	01	01
003	CAM DSP		(L)	5D			FF	18	18
004	CAM DSP	WB_INDOR_G_W	(H)	5E	White balance adjustment value G(3200K)	*	03	00	00
005	CAM DSP		(L)	5F			FF	90	90
006	CAM DSP	WB_R_OUTDOR_W	(H)	5A	White balance adjustment value R(3200K)	*	03	00	00
007	CAM DSP		(L)	5B			FF	D0	DO
008	CAM DSP	WB_B_OUTDOR_W	(H)	5C	White balance adjustment value B(3200K)	*	03	00	00
009	CAM DSP		(L)	5D			FF	92	92
00A	CAM DSP	YDTL_CMPA_W	(H)	16	Y detail enhancer set value, X-axis coordinate of intersection of A and B	*	03	00	00
00B	CAM DSP		(L)	17			FF	1E	1E
00C	CAM DSP	YDTL_CMPB_W	(H)	18	Y detail enhancer set value, X-axis coordinate of intersection of B and C	*	03	00	00
00D	CAM DSP		(L)	19			FF	FA	FA
00E	CAM DSP	YDTL_ADDB_W	(H)	1D	Y detail enhancer set value, y-axis intercept of line B	*	03	00	00
00F	CAM DSP		(L)	1E			FF	00	00
010	CAM DSP	YDTL_ADDC_W	(H)	1F	Y detail enhancer set value, y-axis intercept of line C	*	03	00	00
011	CAM DSP		(L)	20			FF	00	00
012	CAM DSP	YGAM_CMP1_W	(H)	28	Y- γ property set value, X-axis coordinate of intersection of y0 and y1	*	03	00	00
013	CAM DSP		(L)	29			FF	10	10
014	CAM DSP	YGAM_CMP2_W	(H)	2A	Y- γ property set value, X-axis coordinate of intersection of y1 and y2	*	03	00	00
015	CAM DSP		(L)	2B			FF	28	28
016	CAM DSP	YGAM_CMP3_W	(H)	2C	Y- γ property set value, X-axis coordinate of intersection of y2 and y3	*	03	00	00
017	CAM DSP		(L)	2D			FF	40	40
018	CAM DSP	YGAM_CMP4_W	(H)	2E	Y- γ property set value, X-axis coordinate of intersection of y3 and y4	*	03	00	00
019	CAM DSP		(L)		2F		FF	70	70
01A	CAM DSP	YGAM_CMP5_W	(H)	30	Y- γ property set value, X-axis coordinate of int ersection of y4 and y5	*	03	00	00
01B	CAM DSP		(L)	31			FF	AO	AO
01C	CAM DSP	YGAM_CMP6_W	(H)	32	Y- γ property set value, X-axis coordinate of in tersection of y5 and y6	*	03	01	01
01D	CAM DSP		(L)	33			FF	20	20
01E	CAM DSP	YGAM_CMP7_W	(H)	34	Y- γ property set value, X-axis coordinate of in tersection of y6 and y7	*	03	01	01
01F	CAM DSP		(L)	35			FF	C0	00
020	CAM DSP	YGAM_ADD1_W	(H)	3A	Y- γ property set value, data of y-axis intercept of y0	*	01	00	00
021	CAM DSP		(L)	3B			FF	00	00
022	CAM DSP	YGAM_ADD2_W	(H)	3C	Y- γ property set value, data of y-axis intercept of y1	*	01	00	00
023	CAM DSP		(L)	3D			FF	04	04
024	CAM DSP	YGAM_ADD2_W	(H)	3E	Y- γ property set value, data of y-axis intercept of y2	*	01	00	00
025	CAM DSP		(L)	3F			FF	13	13
026	CAM DSP	YGAM_ADD3_W	(H)	40	Y- γ property set value, data of y-axis intercept of y3	*	01	00	00
027	CAM DSP		(L)	41			FF	17	17
028	CAM DSP	YGAM_ADD4_W	(H)	42	Y- γ property set value, data of y-axis intercept of y4	*	01	00	00
029	CAM DSP		(L)	43			FF	2C	2C
02A	CAM DSP	YGAM_ADD5_W	(H)	44	Y- γ property set value, data of y-axis intercept of y5	*	01	00	00
02B	CAM DSP		(L)	45			FF	40	40
02C	CAM DSP	YGAM_ADD6_W	(H)	46	Y- γ property set value, data of y-axis intercept of y6	*	01	00	00
02D	CAM DSP		(L)	47			FF	5B	5B

If you change the setting of a DSP-related data marked with an asterisk, the data will change, being synchronized with VD; if you change the setting of a DSP-related data not marked, the data will immediately change.

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
02E	CAM DSP	YGAM_ADD8_ W (H)	48	Y- γ property set value, data of y-axis intercept of y6 *	01	0C	00
02F	CAM DSP	(L)	49		FF	A8	A8
030	CAM DSP	CSUP_KHL_ W (H)	77	Threshold for color signal suppressing level of luminance signal *	03	02	02
031	CAM DSP	(L)	78		FF	40	40
032	CAM DSP	CSUP_KVEDG_ W (H)	79	Threshold for color signal suppressing level of vertical edge signal *	03	00	00
033	CAM DSP	(L)	7A		FF	20	20
034	CAM DSP	CSUP_KHEDG_ W (H)	7B	Threshold for color signal suppressing level of horizontal edge signal *	03	00	00
035	CAM DSP	(L)	7C		FF	10	10
036	CAM DSP	ENC_CRCC_ CRADATA (H)	BD		3F	10	10
037	CAM DSP	(L)	BE		FF	00	00
038	CAM DSP	ENC_GAIN_ W (H)	EB			00	00
039	CAM DSP	(L)	EC			FF	FF
03A	S-UNIT	YGAM_CMP1_ MEM_ W (H)	28	Y- γ property set value under memory mode, X-axis coordinate of intersection of y0 and y1 *		00	00
03B	S-UNIT	(L)	29			0A	0A
03C	S-UNIT	YGAM_CMP2_ MEM_ W (H)	2A	Y- γ property set value under memory mode, X-axis coordinate of intersection of y1 and y2 *		00	00
03D	S-UNIT	(L)	2B			21	21
03E	S-UNIT	YGAM_CMP3_ MEM_ W (H)	2C	Y- γ property set value under memory mode, X-axis coordinate of intersection of y2 and y3 *		00	00
03F	S-UNIT	(L)	2D			2F	2F
040	S-UNIT	YGAM_CMP4_ MEM_ W (H)	2E	Y- γ property set value under memory mode, X-axis coordinate of intersection of y3 and y4 *		00	00
041	S-UNIT	(L)	2F			3A	3A
042	S-UNIT	YGAM_CMP5_ MEM_ W (H)	30	Y- γ property set value under memory mode, X-axis coordinate of intersection of y4 and y5 *		00	00
043	S-UNIT	(L)	31			99	99
044	S-UNIT	YGAM_CMP6_ MEM_ W (H)	32	Y- γ property set value under memory mode, X-axis coordinate of intersection of y5 and y6 *		01	01
045	S-UNIT	(L)	33			04	04
046	S-UNIT	YGAM_CMP7_ MEM_ W (H)	34	Y- γ property set value under memory mode, X-axis coordinate of intersection of y6 and y7 *		01	01
047	S-UNIT	(L)	35			8E	8E
048	S-UNIT	YGAM_ADD1_ MEM_ W (H)	3A	Y- γ property set value under memory mode, X-axis coordinate of intersection of y0 and y *		00	00
049	S-UNIT	(L)	3B			00	00
04A	S-UNIT	YGAM_ADD2_ MEM_ W (H)	3C	Y- γ property set value under memory mode, X-axis coordinate of intersection of y1 and y *		00	00
04B	S-UNIT	(L)	3D			03	03
04C	S-UNIT	YGAM_ADD3_ MEM_ W (H)	3E	Y- γ property set value under memory mode, X-axis coordinate of intersection of y2 and y *		00	00
04D	S-UNIT	(L)	3F			0C	00
04E	S-UNIT	YGAM_ADD4_ MEM_ W (H)	40	Y- γ property set value under memory mode, X-axis coordinate of intersection of y3and y *		00	00
04F	S-UNIT	(L)	41			29	29
050	S-UNIT	YGAM_ADD5_ MEM_ W (H)	42	Y- γ property set value under memory mode, X-axis coordinate of intersection of y4 and y *		00	00
051	S-UNIT	(L)	43			31	31
052	S-UNIT	YGAM_ADD6_ MEM_ W (H)	44	Y- γ property set value under memory mode, X-axis coordinate of intersection of y5 and y *		00	00
053	S-UNIT	(L)	45			4E	4E
054	S-UNIT	YGAM_ADD7_ MEM_ W (H)	46	Y- γ property set value under memory mode, X-axis coordinate of intersection of y6 and y *		00	00
055	S-UNIT	(L)	47			7F	7F
056	S-UNIT	YGAM_ADD8_ MEM_ W (H)	48	Y- γ property set value under memory mode, X-axis coordinate of intersection of y7 and y *		00	00
057	S-UNIT	(L)	49			D1	D1
058	DEBUG	232C_DATE1_ W (H)		Debugging output 1, RAM address setting		FF	FF
059	DEBUG	(L)				FF	FF
05A	DEBUG	232C_DATE2_ W (H)		Debugging output 2, RAM address setting		FF	FF
05B	DEBUG	(L)				FF	FF
05C	DEBUG	232C_DATE3_ W (H)		Debugging output 3, RAM address setting		FF	FF
05D	DEBUG	(L)				FF	FF
05E	DEBUG	232C_DATE4_ W (H)		Debugging output 4, RAM address setting		FF	FF

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
05F	DEBUG	(L)				FF	FF
060	DEBUG	232C_DATE5_W (H)		Debugging output 5 RAM address setting		FF	FF
061	DEBUG	(L)				FF	FF
062	DEBUG	232C_DATE6_W (H)		Debugging output 6, RAM address setting		FF	FF
063	DEBUG	(L)				FF	FF
064	DEBUG	232C_DATE7_W (H)		Debugging output 7, RAM address setting		FF	FF
065	DEBUG	(L)				FF	FF
066	DEBUG	232C_DATE8_W (H)		Debugging output 8, RAM address setting		FF	FF
067	DEBUG	(L)				FF	FF
068	DEBUG	232C_DATE9_W (H)		Debugging output 9, RAM address setting		FF	FF
069	DEBUG	(L)				FF	FF
06A	DEBUG	232C_DATE10_W (H)		Debugging output 10, RAM address setting		FF	FF
06B	DEBUG	(L)				FF	FF
06C		RESERVE_W (H)		Unused		FF	FF
06D		(L)				FF	FF
06E		RESERVE_W (H)		Unused		FF	FF
06F		(L)				FF	FF
070	ADJ	ADJ_MODE		Adjustment mode setting (00: Signal system, Others: Normal)		FF	FF
071	ADJ	ADJ_SELECT		Adjustment item setting (01: Black balance adjustment)		FF	FF
072	AE_ADJ	AE_CVT		Iris level adjustment value		98	98
073	ADJ	ADJ_CK		For automatic machine adjustment check (for production)		FF	FF
074	DEBUG	BPS_PARM		Baud rate selection		1F	1F
075	MICON	ROM_VERSION		ROM version reading (write-protected)	FF	FF	FF
076	D/A	YGAIN		Y gain adjustment value		FF	FF
077	D/A	CGAIN		C gain adjustment value		FF	FF
078	D/A	RESERVE	CH1			FF	FF
079	D/A	RESERVE	CH2			FF	FF
07A	D/A	RESERVE	CH3			FF	FF
07B	D/A	RESERVE	CH4			FF	FF
07C	D/A	RESERVE	CH5			FF	FF
07D	D/A	RESERVE	CH6			FF	FF
07E	D/A	RESERVE	CH7			FF	FF
07F	D/A	RESERVE	CH8			FF	FF
080	D/A	RESERVE	CH9			FF	FF
081	D/A	RESERVE	CH10			FF	FF
082	D/A	RESERVE	CH11			FF	FF
083	D/A	RESERVE	CH12			FF	FF
084	D/A	RESERVE	CH1			FF	FF
085	D/A	RESERVE	CH2			FF	FF
086	D/A	RESERVE	CH3			FF	FF
087	D/A	RESERVE	CH4			FF	FF
088	D/A	RESERVE	CH5			FF	FF
089	D/A	RESERVE	CH6			FF	FF
08A	D/A	RESERVE	CH7			FF	FF
08B	D/A	RESERVE	CH8			FF	FF
08C	D/A	RESERVE	CH9			FF	FF
08D	D/A	RESERVE	CH10			FF	FF
08E	D/A	RESERVE	CH11			FF	FF
08F	D/A	RESERVE	CH12			FF	FF

ADRS	PART	LABEL	DSP ADRS	Description		MAX	NTSC	PAL
090	CAM DSP	MAT_KBG_ P	84	R-Y phase adjustment (+)	✻▲4	FF	49	49
091	CAM DSP	MAT_KBG_M	85	R-Y phase adjustment (-)	✻	FF	52	52
092	CAM DSP	MAT_KRG_ P	86	B-Y phase adjustment (+)	✻▲4	FF	19	19
093	CAM DSP	MAT_KRG_ M	87	B-Y phase adjustment (-)	✻	FF	OD	OD
094	CAM DSP	DIFGAIN_GBY_ P	88	B-Y gain adjustmen (B-Y ≧ 0)	✻▲4	7F	29	29
095	CAM DSP	DIFGAIN_GBY_ M	89	B-Y gain adjustment (B-Y < 0)	✻	7F	16	16
096	CAM DSP	DIFGAIN_GBY_ P	8A	R-Y gain adjustment (R-Y ≧ 0)	✻▲4	7F	39	39
097	CAM DSP	DIFGAIN_GBY_ M	8B	B-Y gain adjustment (R-Y < 0)	✻	7F	2B	2B
098	CAM DSP	ENC_BFMIX_ SEYUP	C2	Burst signal gain adjustment value		FF	26	26
099	CAM DSP	OBLPF_MODE (SFTK)	10	Selection of OB clamp types		OF	08	08
09A	CAM DSP	RAM_TEST	11	RAM TEST		7F	00	00
09B	CAM DSP	OBLEVELO (OBSET1)	12	OB level adjustment 1	✻	7F	20	20
09C	CAM DSP	OBLEVEL1 (OBSET2)	13	OB level adjustment 2	✻	7F	20	20
09D	CAM DSP	OBOFFSETO (LCLIPSET1)	14	Video period level adjustment of luminance signal 1	✻	7F	00	00
09E	CAM DSP	OBOFFSET1 (LCLIPSET2)	15	Video period level adjustment of luminance signal 2	✻	7F	00	00
09F	CAM DSP	YDTL_MLTA	1A	Y detail enhancer set value, setting of gradient of A	✻	OF	08	08
0AO	CAM DSP	YDTL_MLTB	1B	Y detail enhancer set value, setting of gradient of B	✻	OF	08	08
0A1	CAM DSP	YDTL_MLTC	1C	Y detail enhancer set value, setting of gradient of C	✻	OF	08	08
0A2	CAM DSP	YDTL_TEST	21	Y detail enhancer TEST MODE		FF	00	00
0A3	CAM DSP	HDTL_GAIN_H	22	Horizontal edge signal addition rate	✻▲4	OF	89	44
0A4	CAM DSP	HDTL_GAIN_L	23	Horizontal edge signal addition rate	✻▲4	OF	22	33
0A5	CAM DSP	VDTL_GAIN	24	Vertical edge signal addition rate	✻▲2	OF	BC	BC
0A6	CAM DSP	NCLIP_ZEVEL	25	Noise clip level	▲2		07	08
0A7	CAM DSP	NCLIP_SHIFT	26	NCLIP shift amount	✻	03	00	00
0A8	CAM DSP	YHMIX_TEST	27	YH_MiX TEST MODE		FF	03	03
0A9	CAM DSP	YGAM_MLT12	36	Y- γ property set value, setting of gradient of y0 and y1	✻	FF	B9	B9
0AA	CAM DSP	YGAM_MLT34	37	Y- γ property set value, setting of gradient of y2 and y3	✻	FF	6B	6B
0AB	CAM DSP	YGAM_MLT56	38	Y- γ property set value, setting of gradient of y4 and y5	✻	FF	8C	8C
0AC	CAM DSP	YGAM_MLT78	39	Y- γ property set value, setting of gradient of y6 and y7	✻	FF	97	97
0AD	CAM DSP	YDLY	4A	Y DELAY	✻▲2	1F	05	12
0AE	CAM DSP	YFADE_GYFADE	4B	Setting of luminance signal component gain at fading	✻▲2	3F	2A	30
0AF	CAM DSP	YFADE_KYFADE	4C	Setting of luminance component offset level at fading	✻	FF	00	00
0B0	CAM DSP	RAM_BLKM	4F			1C	1C	
0B1	CAM DSP	CSEP_KR	56	Color separation coefficient R		3F	12	12
0B2	CAM DSP	CSEP_KB	57	Color separation coefficient B		3F	1A	1A
0B3	CAM DSP	CSEP_KG	56	Color separation coefficient G		3F	18	18
0B4	CAM DSP	CSEP_SPL_STL	59	Timing of input signal and thres in CSEP circuit		1F	13	13
0B5	CAM DSP	CGAIN_BBB	60	Black balanceR	✻	FF	CC	CC
0B6	CAM DSP	CGAIN_BBB	61	Black balanceB	✻	FF	C7	C7
0B7	CAM DSP	CGAIN_BBG	62	Black balance G	✻	FF	BA	BA
0B8	CAM DSP	CGAM_CMP_HIGH	63	C- γ property set value, most significant bit of CMP1, 2, 3, 4, 5, 6, 7		FF	00	00
0B9	CAM DSP	CGAM_CMP1	64	C- γ property set value, X-axis coordinate of intersection of y0 and y1		FF	08	08
08A	CAM DSP	CGAM_CMP2	65	C- γ property set value, X-axis coordinate of intersection of y1 and y2		FF	18	18
08B	CAM DSP	CGAM_CMP3	66	C- γ property set value, X-axis coordinate of intersection of y2and y3		FF	30	30
08C	CAM DSP	CGAM_CMP4	67	C- γ property set value, X-axis coordinate of intersection of y3 and y4		FF	48	48
08D	CAM DSP	CGAM_CMP5	68	C- γ property set value, X-axis coordinate of intersection of y4 and y5		FF	60	60
08E	CAM DSP	CGAM_CMP6	69	C- γ property set value, X-axis coordinate of intersection of y5 and y6		FF	A0	A0
08F	CAM DSP	CGAM_CMP7	6A	C- γ property set value, X-axis coordinate of intersection of y6 and y7		FF	E0	E0
0C0	CAM DSP	CGAM_CMP01	6B	C- γ property set value, setting of gradient of y0 and y1	✻	FF	87	87

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
0C1	CAM DSP	CGAM_CMP23	6B	C- γ property set value, setting of gradient of y2 and y3 *	FF	6B	6B
0C2	CAM DSP	CGAM_CMP45	6D	C- γ property set value, setting of gradient of y4 and y5 *	FF	9C	9C
0C3	CAM DSP	CGAM_CMP67	6E	C- γ property set value, setting of gradient of y6 and y7 *	FF	96	96
0C4	CAM DSP	CGAM_ADD0	6F	C- γ property set value, data of y-axis intercept of y0 *	FF	00	00
0C5	CAM DSP	CGAM_ADD1	70	C- γ property set value, data of y-axis intercept of y1 *	FF	01	01
0C6	CAM DSP	CGAM_ADD2	71	C- γ property set value, data of y-axis intercept of y2 *	FF	04	04
0C7	CAM DSP	CGAM_ADD3	72	C- γ property set value, data of y-axis intercept of y3 *	FF	07	07
0C8	CAM DSP	CGAM_ADD4	73	C- γ property set value, data of y-axis intercept of y4 *	FF	10	10
0C9	CAM DSP	CGAM_ADD5	74	C- γ property set value, data of y-axis intercept of y5 *	FF	22	22
0CA	CAM DSP	CGAM_ADD6	75	C- γ property set value, data of y-axis intercept of y6 *	FF	31	31
0CB	CAM DSP	CGAM_ADD7	76	C- γ property set value, data of y-axis intercept of y7 *	FF	5B	5B
0CC	CAM DSP	CGAM_GHL	7D	Setting of color signal suppressing rate of luminance signal *	FF	90	90
0CD	CAM DSP	CGAM_GVEDG	7E	Setting of color signal of vertical edge signal suppressing rate of luminance signal *	FF	28	28
0CE	CAM DSP	CGAM_GVEDG	7F	Setting of color signal of horizontal edge signal suppressing rate of luminance signal *	FF	40	40
0CF	CAM DSP	CGAM_CUPV	82	CSUP_VDTL, timing setting	7F	03	03
0D0	CAM DSP	DIFCGAIN_CTL	8C	2PARAM, 4PARAM mode selection, color noise clip	07	04	04
0D1	CAM DSP	CFADE_GVFADE	8E	Setting of color signal component gain at fading *	3F	3F	3F
0D2	CAM DSP	RY_OFFSET	8F	▲7		04	00
0D3	CAM DSP	BY_OFFSET	90	▲4		01	00
0D4	CAM DSP	TEST_T1	98	C-system DSP test mode control 1	FF	00	00
0D5	CAM DSP	TEST_T2	99	C-system DSP test mode control2	FF	00	00
0D6	CAM DSP	TEST_T3	9A	C-system DSP test mode control 3	FF	00	00
0D7	CAM DSP	TEST_T4	9B	C-system DSP test mode control 4	FF	00	00
0D8	CAM DSP	SSG_MODE	9C	SSG mode selection (Write-regulated)	FF	80	89
0D9	CAM DSP	SSG_DBCP_SP	9D	OBCP rising edge phase adjustment	7F	04	04
0DA	CAM DSP	SSG_DBCP_SN	9E	OBCP falling edge phase adjustment	7F	04	04
0DB	CAM DSP	SSG_DBCP_SP	9F	PBLK rising edge phase adjustment	7F	06	06
0DC	CAM DSP	SSG_DBCP_SN	A0	PBLK falling edge phase adjustment	7F	06	06
0DD	CAM DSP	SSG_HG_S	A1	HG phase adjustment	7F	01	01
0DE	CAM DSP	SSG_HSYNC_SP	A2	HSYNC rising edge phase adjustment	7F	3C	45
0DF	CAM DSP	SSG_HSYNC_SN	A3	HSYNC falling edge phase adjustment	7F	3C	45
0E0	CAM DSP	SSG_VSYNC_S	A4	VSYNC phase adjustment	7F	3C	45
0E1	CAM DSP	SSG_CBLK_SP	A5	CCBLK rising edge phase adjustment	7F	3D	46
0E2	CAM DSP	SSG_CBLK_SN	A6	CCBLK falling edge phase adjustment	7F	3B	42
0E3	CAM DSP	SSG_CSYNC_SP	A7	SYNC rising edge phase adjustment	7F	37	42
0E4	CAM DSP	SSG_CSYNC_SN	A8	SYNC falling edge phase adjustment	7F	3A	42
0E5	CAM DSP	SSG_BF_SP	A9	BFP rising edge phase adjustment	7F	3C	44
0E6	CAM DSP	SSG_BF_SN	AA	BFP falling edge phase adjustment	7F	3B	44
0E7	CAM DSP	SSG_LSW_S	AB	LSW phase adjustment	7F	43	43
0E8	CAM DSP	SSG_CRCC_S	AC	CRCC phase adjustment	7F	43	43
0E9	CAM DSP	SSG_TEST	AD	SSG TEST MODE	FF	80	80
0EA	CAM DSP	TG_MODE	AE	TG mode selection ▲2	FF	24	05
0EB	CAM DSP	SRC_TST	AF	SRC TEST	01	00	00
0EC	CAM DSP	SSG_ETC	B0			18	18
0ED	CAM DSP	TG_PS	B1			00	00
0EE	CAM DSP	ENC_TEST_SEL	BA	Encoder test		00	00
0EF	CAM DSP	SYNCMIX_KSETUP	BB	Set-up level adjustment value *▲7	3F	46	42
0F0	CAM DSP	SYNCMIX_KSYNC	BC	Pedestal level setting (sink chip ~ pedestal)	3F	43	43
0F1	CAM DSP	ENC_CRCC_CRLEVEL	BF		FF	C0	C0

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
0F2	CAM DSP	ENC_CRCC_CRLEVELB	CO			49	49
0F3	CAM_DSP	ENC_YOUT_DELAY	C1	Y-OUT DELAY		86	86
0F4	D_AUTO	AF_CMPA	C4	Comparative value a of AF	FF	25	25
0F5	D_AUTO	AF_CMPB	C5	Comparative value b of AF	FF	3B	3B
0F6	D_AUTO	AF_CMPC	C6	Comparative value c of AF	FF	CC	CC
0F7	D_AUTO	AF_CMPD	C7	Comparative value d of AF	FF	90	90
0F8	D_AUTO	AF_MULAB	C8	Coefficient of γ of AF (Upper 4 bits: Coefficient of b. Lower 4 bits: Coefficient of a)	FF	8B	8B
0F9	D_AUTO	AF_MULCD	C9	Coefficient of γ of AF (Upper 4 bits: Coefficient of d. Lower 4 bits: Coefficient of c)	FF	A9	A9
0FA	D_AUTO	AF_MULXE	CA	Coefficient of γ of AF (Lower 4 bits:coefficient of)Comparative value of γ of AF	FF	84	84
0FB	D_AUTO	AF_ADDB	CB	Added value of b of γ for AF	FF	0E	0E
0FC	D_AUTO	AF_ADDC	CC	Added value of c of γ for AF	FF	28	28
0FD	D_AUTO	AF_ADDD	CD	Added value of d of γ for AF	FF	5B	5B
0FE	D_AUTO	AF_ADDE	CE	Added value of e of γ for AF	FF	BF	BF
0FF	D_AUTO	AF_NS_EIDE	CF	Noise slice value of wide band	FF	01	01
100	D_AUTO	AF_NS_NALL	D0	Noise slice value of narrow band	FF	02	02
101	D_AUTO	AF_NS_POSI	D1	Horizontal position of AF frame	FF	15	15
102	D_AUTO	AF_NS_SIZE	D2	Horizontal width of AF frame	FF	7E	7E
103	D_AUTO	AF_NS_POSI	D3	Vertical position of AF frame	FF	1C	1C
104	D_AUTO	AF_NS_SIZE	D4	Vertical width of AF frame	FF	A8	AB
105	D_AUTO	AF_LEVEL	D5		FF	FF	FF
106	D_AUTO	AF_YH_PRE	D6		FF	01	01
107	D_AUTO	AF_YH_POST	D7		FF	1E	1E
108	D_AUTO	WB_IQK	D8	Conversion coefficient of iq axis conversion of WB (Upper 4 bits: α , Lower 4 bits: β)	FF	79	79
109	D_AUTO	WB_I0	D9	I axis limit value min. of WB ▲9	FF	EE	EE
10A	D_AUTO	WB_I1	DA	I axis limit value max. of WB	FF	24	24
10B	D_AUTO	WB_I2	DB	I axis offset value of WB	FF	00	00
10C	D_AUTO	WB_Q0	DC	Q axis limit value min. of WB	FF	FA	FA
10D	D_AUTO	WB_Q1	DD	Q axis limit value max. of WB	FF	08	08
10E	D_AUTO	WB_Q2	DE	Q axis offset value of WB	FF	00	00
10F	D_AUTO	WB_YHL	DF	YH limit value min. of WB	FF	60	60
110	D_AUTO	WB_YHH	E0	D-AUTO horizontal position adjustment	FF	FF	FF
111	D_AUTO	DA_HDLY	E1	YH limit value min. of WB	FF	8E	8E
112	D_AUTO	AF_HDLY	E2	Horizontal position adjustment of AF	FF	32	32
113	D_AUTO	AE_HDLY	E3	Horizontal position adjustment of AE	FF	4E	4E
114	D_AUTO	WB_HDLY	E4	Horizontal position adjustment of WB	7F	27	27
115	D_AUTO	DAUTO_MODE_A	E5	D-AUTO mode switch A	7F	3C	44
116	D_AUTO	DAUTO_MODE_B	E6	D-AUTO mode switch B	7F	3B	44
117	CAM DSP	TOTORO_ETC1	E7	Camera DSP mode switch	7F	43	43
118	CAM DSP	TOTORO_ETC2	E8	Camera DSP mode switch	7F	43	43
119	CAM DSP	TOTORO_ETC3	E9	Camera DSP mode switch ▲3	FF	80	80
11A	CAM DSP	TOTORO_ETC4	EA	Camera DSP mode switch	FF	24	05
11B	CAM DSP	DA_DMONI	F0	D-AUTO monitor output switch	01	00	00
11C	D_AUTO	TM1_MODE	F1	D-AUTO test mode		18	18
11D	D_AUTO	TM2_MODE	F2	D-AUTO test mode		00	00
11E	D_AUTO	TM3_MODE	F3	D-AUTO test mode		00	00
11F	S_UNIT	YGAM_MLT12_MEM	36	Y- γ characteristic setting value in the memory mode. Inclination setting of y0, y1 *	3F	46	42
120	S_UNIT	YGAM_MLT34_MEN	37	Y- γ characteristic setting value in the memory mode. Inclination setting of y2, y3 *	FF	BC	BC
121	S_UNIT	YGAM_MLT56_MEN	38	Y- γ characteristic setting value in the memory mode. Inclination setting of y4, y5 *	FF	AE	AE
122	S_UNIT	YGAM_MLT78_MEN	39	Y- γ characteristic setting value in the memory mode. Inclination setting of y6, y7 *	FF	83	83

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
123	S_UNIT	ENC_BFMIX_SETUP_MEN	C2	Set value of burst signal gain under memory mode	FF	20	26
124	S_UNIT	CGAIN_OFFSET_MEN		CGAIN offset value under memory mode	FF	00	00
125	S_UNIT	CFADE_GCFADE_MEN	8E	Setting of color signal component gain at fading under memory mode *	3F	3F	3F
126	S_UNIT	LL_CFADE_MIN_MEN		Low illuminance normal color suppressing minimum level under memory mode		28	2F
127	S_UNIT	LL_CFADE_GUP_MEN		Low illuminance gain-up color suppressing minimum level under memory mode		1C	2C
128	S_UNIT	HDTL_H_GAIN_MEN	22	Horizontal edge signal addition rate *	0F	44	44
129	S_UNIT	HDTL_L_GAIN_MEN	23	Horizontal edge signal addition rate *	0F	33	33
12A	S_UNIT	VDTL_MEN	24	Vertical edge signal addition rate *	0F	CC	CC
12B	AWB	WB_OFSTTW_R		R offset amount under twilight mode		10	18
12C	AWBT	WB_OFSTTW_B		B offset amount under twilight mode		DF	DF
12D	AWB	WB_OFST_START				28	28
12E	AWB	WB_YHL_MIN		▲5		50	50
12F	AWB	WB_YHL_INI				60	60
130	AWB	WB_SLANT_F1				80	80
131	AWB	WB_INI_TIME		White balance initialization (high-speed operation) time		78	64
132	AWB	WB_OUTDOOR_I		Threshold for deviation amount in +I direction to judge outdoor environment		05	05
133	AWB	WB_IREF		Automatic white balance operation reference level I		02	12
134	AWB	WB_QREF		Automatic white balance operation reference level Q		0C	06
135	AWB	WB_R2MAX_3		Max. value of outdoor R 2biaxial compensation range		1A	15
136	AWB	WB_R2MAX_3		Max. value of outdoor B 2biaxial compensation range		1A	10
137	AWB	resetL_vcr				80	80
138	AWB	WB_OUTDOOR_AREA_R		Outdoor mode operation area R		50	50
139	AWB	WB_OUTDOOR_AREA_BL		Outdoor mode operation area B_L		A0	A0
13A	AWB	WB_OUTDOOR_AREA_BH		Outdoor mode operation area B_H		60	60
13B	AWB	WB_OFST56_L		Outdoor mode 5600 K offset value L		10	10
13C	AWB	WB_OFST56_H		Outdoor mode 5600 K offset valueH ▲7		00	00
13D	AWB	WB_ADMT_PUSHAUTO_I		Admitted level in I direction at PUSHAUTO		10	10
13E	AWB	WB_ADMT_PUSHAUTO_Q		Admitted level in Q direction at PUSHAUTO		10	10
13F	AWB	WB_SHFT_FL		F2 (fluorescent lamp) shift amount ▲9		50	50
140	AWB	WB_SHFT_OUT		F3 (outdoor)shift amount ▲3		F0	F0
141	AWB	WB_IRIS_OPEN		Iris open level of fuzzy inference		50	50
142	AWB	WB_IRIS_CLOSE		Iris close level of fuzzy inference		C0	C0
143	AWB	WB_U2_HIGH				80	80
144	AWB	WB_IRIS_OFFSET		For detection of condition change		30	30
145	AWB	WB_ADMT_I		Admitted level in I direction		08	08
146	AWB	WB_ADMT_Q		Admitted level in Q direction		08	08
147	AWB	WB_RESTART_I		Restart level in I direction		34	34
148	AWB	WB_AREA_DISABLE		Area distinction Q-axis direction dead zone		40	80
149	CAM DSP	MAT_COMPE_BP		Compensation of high color temperature color repeatability ▲2		8D	D3
14A	CAM DSP	MAT_COMPE_BM		Compensation of high color temperature color repeatability ▲2		12	01
14B	CAM DSP	MAT_COMPE_RP		Compensation of high color temperature color repeatability ▲2		24	40
14C	CAM DSP	MAT_COMPE_RM		Compensation of high color temperature color repeatability ▲5		02	F4
14D	CAM DSP	DCGAIN_COMPE_BYP		Compensation of high color temperature color repeatability ▲2		FB	01
14E	CAM DSP	DCGAIN_COMPE_BYM		Compensation of high color temperature color repeatability ▲2		10	FE
14F	CAM DSP	DCGAIN_COMPE_RYP		Compensation of high color temperature color repeatability ▲2		12	FE
150	CAM DSP	DCGAIN_COMPE_RYM		Compensation of high color temperature color repeatability		OD	F6
151	AWB	WB_DARK_L		Mean level to judge light shielding		08	08
152	AWB	WB_DARK_H		Mean level to judge complete light shielding		10	10
153		poff_ok_wait		CAM power supply OFF delay timer		0A	0A

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
154		r_vd_standy				16	16
155	AWB	WB_SELECT_SW		WB function selection SW		DF	DF
156	AWB	RESERVE				FF	FF
157	AWB	RESERVE				FF	FF
158	AWB	RESERVE				FF	FF
159	AWB	WB_INDOOR_I		Threshold for deviation amount in +I direction to judge outdoor environment		30	30
15A	AWB	RESERVE				FF	FF
15B	AWB	RESERVE				FF	FF
15C	AWB	RESERVE				FF	FF
15D	AWB	WB_AE_LIMIT				20	20
15E	AWB	RESERVE				FF	FF
15F	AWB	WB_SHIFT_F1		F1 (halogen) shift amount		20	30
160	AWB	RESERVE				FF	FF
161	AWB	WB_U3_HIGH		▲5		C0	C0
162	AWB	WB_WEIGHT_I		White balance center area weighting		80	80
163	AWB	WB_STEP1		White balance operation step 1		C0	C0
164	AWB	WB_STEP2		White balance operation step 2		A0	A0
165	AWB	WB_STEP3		White balance operation step 3		10	10
166	AWB	WB_IREF_PUSHAOUTO		White balance operation reference level I at PUSHAUTO ▲4		08	12
167	AWB	WB_QREF_PUSHAOUTO		White balance operation reference level Q at PUSHAUTO ▲4		08	06
168	AWB	WB_IRIS_MAN		Iris data offset under iris shift mode		18	18
169	AWB	WB_R2MAX_2		Max. value in R biaxial compensation range using fluorescent lamp		18	20
16A	AWB	WB_B2MAX_2		Max. value in B2 iaxial compensation range using fluorescent lamp		18	20
16B	AWB	WB_RB2MAX_1		Max. value in biaxial compensation range using halogen		0D	0D
16C	AWB	WB_STEP_OUTDOOR		WB operation step under outdoor mode		40	40
16D	AWB	BYM_PERCENT		Ratio of B-Y gain (-) against B-Y gain (+) (1:1 at 80) ▲2		72	81
16E	AWB	RYM_PERCENT		Ratio of R-Y gain (-) against R-Y gain (+) (1:1 at 80) ▲2		87	88
16F	AWB	WB_OK_EEP				01	01
170	AWB	PUSHAOUT_R2_MAX		Max. value of R biaxial compensation at PUSHAUTO		7F	7F
171	AWB	PUSHAOUT_B2_MAX		Max. value of B biaxial compensation at PUSHAUTO		7F	7F
172	AWB	WB_I0_LOW		Gate area IO min. value ▲5		FE	FE
173	AWB	WB_I0_HIGHT		Gate area IO max. value		F8	F8
174	AWB	WB_I1_LOW		Gate area I1 min. value		10	10
175	AWB	WB_I1_HIGH		Gate area I1 max. value		24	24
176	AWB	WB_PIXEL_H		Integral pixel threshold for raising low luminance gate		20	20
177	AWB	WB_PIXEL_L		Integral pixel threshold for lowering low luminance gate		10	10
178	AWB	PIXEL_LOCK		Threshold for judging less number of integral pixels		00	10
179	AWB	BY_MAT_PRESENT		Ratio of B-Y phase (-) against B-Y phase (+)(1:1 at 80) ▲2		36	5A
17A	AWB	RY_MAT_PRESENT		Ratio of R-Y phase (-) against R-Y phase (+)(1:1 at 80) ▲2		28	5A
17B	NOISEADJ	nosadj_timer		AF noise adjustment time		3C	3C
17C	AWB	WB_DIFF1		WB deviation threshold		40	40
17D	AWB	WB_DIFF2		WB deviation threshold		12	12
17E	AWB	WB_DIFF3		WB deviation threshold		80	80
17F	AWB	WB_DIFF4		WB deviation threshold		80	80
180	AWB	WB_DIFF5		WB deviation threshold		18	18
181	AWB	WB_DIFF6		WB deviation threshold		06	06
182	AWB	GBY_MEM_OFFSET_P				00	00
183	AWB	GRY_MEM_OFFSET_P				00	00
184	AWB	RESERVE				FF	FF

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
185	AWB	RESERVE				FF	FF
186	AWB	RESERVE				FF	FF
187	AWB	RESERVE				FF	FF
188	AE	AGC_FILTER		Filter for operating AGC at the same speed as iris		02	02
189	AE	CFT_WM		Ratio of weighted mean and peak value ▲3	55	32	32
18A	AE	CFT_WM_PT		Ratio of weighted mean and peak value under party mode	55	28	28
18B	AE	CFT_WM_SKI		Ratio of weighted mean and peak value under skiing mode	55	4E	4E
18C	AE	CFT_WM_TW		Ratio of weighted mean and peak value under twilight mode(Under memory mode)	55	36	36
18D	AE	CFT_WM_MEM		Ratio of weighted mean and peak value(Under memory mode)	55	32	32
18E	AE	CFT_WM_PT_MEM		Ratio of weighted mean and peak value under party mode(Under memory mode)	55	28	28
18F	AE	CFT_WM_SKI_MEM		Ratio of weighted mean and peak value under skiing mode(Under memory mode)	55	4E	4
190	AE	CFT_WM_TW_MEM		Ratio of weighted mean and peak value under twilight mode(Under memory mode)	55	36	36
191	AE	AE_CVT_OFST_PT		Luminance level conversion offset value under party mode		0A	0A
192	AE	AE_CVT_OFST_SKI		Luminance level conversion offset value under skiing mode		F4	F4
193	AE	AE_CVT_OFST_TW		Luminance level conversion offset value under twilight mode		F0	F0
194	AE	AE_CVT_OFST_PT_MEM		Luminance level conversion offset value under party mode(Under memory mode)		0A	0A
195	AE	AE_CVT_OFST_SKI_MEM		Luminance level conversion offset value under skiing mode(Under memory mode)		F4	F4
196	AE	AE_CVT_OFST_TW_MEM		Luminance level conversion offset value under twilight mode(Under memory mode)		F0	F0
197	AE	AE_ERROR1		AE operation speed changeover position 1		01	01
198	AE	AE_ERROR2		AE operation speed changeover position 2		04	04
199	AE	AE_ERROR3		AE operation speed changeover position 3		0A	0A
18A	AE	AE_STEP_GAIN0		Speed of low-speed mode ▲3		04	04
19B	AE	AE_STEP_GAIN1		Speed of intermediate to low-speed mode ▲3		0C	0C
19C	AE	AE_STEP_GAIN2		Speed of intermediate to high-speed mode ▲3		15	15
19D	AE	AE_STEP_GAIN3		Speed of high-speed mode ▲3		80	80
19E	AE	PERK_WEIGFT		Weighting of peak value in areas outside the center and lower areas		C0	C0
19F	AE	AE_REF_RATE		Change amount of reference value when iris is under manual mode		OF	OF
1A0	AE	IRIS_CLOSE		D/A output value when iris is close (adjustment data)		90	90
1A1	AE	AE_UWT0		Weighted mean coefficient for AE control (upper area) ▲3		03	03
1A2	AE	AE_UWT1		Weighted mean coefficient for AE control (lower area) ▲3		6A	6A
1A3	AE	AE_UWT2		Weighted mean coefficient for AE control (center area)		5B	5B
1A4	AE	AE_UWT3		Weighted mean coefficient for AE control (both ends of center area)		38	38
1A5	AE	AE_UWT0_SKI		Weighted mean coefficient for AE control under skiing mode(upper area)		30	30
1A6	AE	AE_UWT1_SKI		Weighted mean coefficient for AE control under skiing mode (lower area)		50	50
1A7	AE	AE_UWT2_SKI		Weighted mean coefficient for AE control(center area)		50	50
1A8	AE	AE_UWT3_SKI		Weighted mean coefficient for AE control (both ends of center area)		30	30
1A9	AE	BLC_DATA		Fixed compensation data when counterlight compensation SW is ON		10	10
1AA	AE	BLC_DATA_SKI		Compensation data when counterlight compensation SW is ON (skiing mode)		08	08
1AB	AE	BLC_DATA_TW		Compensation data when counterlight compensation SW is ON (twilight mode)		0A	0A
1AC	AE	BLC_DATA_PT		Compensation data when counterlight compensation SW is ON (party mode)		10	10
1AD	AE	BLC_DATA_SP		Compensation data when counterlight compensation SW is ON (sports mode)		10	10
1AE	AE	FLK_GAIN_MAX		Flickering compensation gain		08	08
1AF	AE	FLK_ERROR		Error prevention parameter when flickering		30	30
1B0	AE	EXP_11		Exposure control value when iris is at MID1		38	38
1B1	AE	EXP_12		Exposure control value when iris is at MID2		78	78
1B2	AE	EXP_13		Exposure control value when iris is at MID3		A2	A2
1B3	AE	EXP_14		Exposure control value when iris is open		D0	D0
1B4	AE	IRIS1_WT		Iris MID1 set value		F3	F3
1B5	AE	IRIS2_WT		Iris MID2 set value		CE	CE

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
1B6	AE	IRIS3_WT		Iris MID3 set value		A3	A3
1B7	AE	AE_LOCK_ON		Value for turning on AE lock (deviation amount from reference value, lower 8 bits)		40	40
1B8	AE	AE_LOCK_OFF		Value for turning off AE lock (deviation amount from reference value, upper 8 bits)		01	01
1B9	AE	AE_SHUT_ON				C0	C0
1BA	AE	AE_SHUT_MAX				00	00
1BB	AE	RESERVE		Unused		FF	FF
1BC	AE	RESERVE		Unused		FF	FF
1BD	AE	RESERVE		Unused		FF	FF
1BE	AE	RESERVE		Unused		FF	FF
1BF	AE	RESERVE		Unused		FF	FF
1C0	AE	RESERVE		Unused		FF	FF
1C1	AE	AGC_MIN		AGC min. value		33	33
1C2	AE	AGC_MAX		D/A output value when AGC is max. ▲2		A0	AA
1C3	AE	AGC_MAX_TW		D/A output value when AGC is max. under twilight mode		50	50
1C4	AE	GAIN_UP_STEP		1VD gain-up amount under gain-up mode		50	50
1C5	AE	GAIN_UP_MAX		Max. value of addition amount data (upper eight bits) under gain-up mode		26	26
1C6	AE	AGC_SUP_START		AGC suppression start point		88	88
1C7	AE	AGC_SUP_RATE		AGC suppression rate		A8	A8
1C8	AE	AE_SHUTTER_START		Shutter start iris position (set by r_iris value)		F0	F0
1C9	AE	AE_SHUTTER_END		Shutter end iris position (set by r_iris value)		FF	FF
1CA	AE	AE_SHUTTER_MAX1		Max. value of shutter speed at portrait		05	05
1CB	AE	AE_ASHUTTER_MAX2		Max. value of shutter speed between shutter start and shutter end		00	00
1CC	AE	AE_TEST		AE test mode		FF	FF
1CD	AE	IRIS_H		ME mode iris control output (upper)		FF	FF
1CE	AE	IRIS_L		ME mode iris control output (lower)		FF	FF
1CF	AE	AGC_H		ME mode AGC control output (upper)		FF	FF
1D0	AE	AGC_L		ME mode AGC control output (lower)		FF	FF
1D1	AE	IRIS_ZM_OFFSET		Iris opening position offset parameter, depending on zooming position		00	00
1D2	AE	KNEE_POINT_LMT		Setting of knee point control start point (contrast ratio)		FF	FF
1D3	AE	RESERVE				FF	FF
1D4	AE	RESERVE				FF	FF
1D5	AE	RESERVE				FF	FF
1D6	AE	RESERVE				FF	FF
1D7	AE	RESERVE				FF	FF
1D8	C/B	OB_REF		OB control convergent point (00H to 40H)		20	20
1D9	C/B	OB_ADMT		OB control admitted range (The value 4 times this value is the restart level.)		10	10
1DA	C/B	BBAL_ADMT		Black balance control restart level		01	01
1DB	C/B	BBAL_ADJ_R_ADMT1		Black balance automatic adjustment R admitted range (when AGC is min.)		2A	2A
1DC	C/B	BBAL_ADJ_B_ADMT1		Black balance automatic adjustment B admitted range(when AGC is min.)		38	38
1DD	C/B	BBAL_ADJ_R_ADMT2		Black balance automatic adjustment R admitted range (when AGC is max. under gain-up mode)		70	70
1DE	C/B	BBAL_ADJ_B_ADMT2		Black balance automatic adjustment B admitted range (when AGC is max. under gain-up mode)		80	80
1DF	C/B	ROB_OFST1_OUT		Offset value for ROB measurement when AGC is min. (outdoor)		FF	FF
1E0	C/B	ROB_OFST2_OUT		Offset value for ROB measurement when AGC is max (outdoor)		FF	FF
1E1	C/B	ROB_OFST3_OUT		Offset value for ROB measurement (when AGC is max.) under gain-up mode (outdoor)		00	00
1E2	C/B	ROB_OFST1_OUT		Offset value for BOB measurement when AGC is min.(outdoor)		FF	FF
1E3	C/B	ROB_OFST2_OUT		Offset value for BOB measurement when AGC is max.(outdoor)		FF	FF
1E4	C/B	ROB_OFST3_OUT		Offset value for ROB measurement (when AGC is max.) under gain-up mode (outdoor)		FF	FF
1E5	C/B	ROB_OFST1		Offset value for ROB measurement when AGC is min.		FF	FF
1E6	C/B	ROB_OFST2		Offset value for ROB measurement when AGC is max.		FF	FF

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
1E7	C/B	ROB_OFST3		Offset value for ROB measurement (when AGC is max.) under gain-up mode		FF	FF
1E8	C/B	ROB_OFST1		Offset value for BOB measurement when AGC is min.		FF	FF
1E9	C/B	ROB_OFST2		Offset value for BOB measurement when AGC is max		FF	FF
1EA	C/B	ROB_OFST3		Offset value for BOB measurement (when AGC is max.) under gain-up mode		FF	FF
1EB	C/B	AD_REF				7F	7F
1EC	SYNC	ssg_hsync_sp_receive		Display position compensation value when SU3 is received ▲6		28	31
1ED	SYNC	ssg_hsync_sn_receive		Display position compensation value when SU3 is received ▲6		28	31
1EE	SYNC	ssg_hsync_s_receive		Display position compensation value when SU3 is received ▲6		28	31
1EF	E-ZOOM	FADE_RVCTLD				00	00
1F0	E-ZOOM	FADE_TIME		Fading time when Power is ON		F0	F0
1F1	E-ZOOM	FADE_CTL		Fade control		3F	3F
1F2	E-ZOOM	FADE_LEVEL		Fade level		00	00
1F3	MICON	MODE_SELECT		Mode selection setting		FF	FB
1F4	MICON	MODE_CTL0		Mode selection setting		EF	EF
1F5	ZOOM	ZOOM_SPEED_SELECT		Selection of zooming speed under high-speed zooming mode		06	06
1F6	ZOOM	PB_ZOOM_SPEED_SELECT		Selection of zooming speed under play zooming mode		06	06
1F7	MICON	vcrcam_delay_thresh		CAM-H signal delay counter when switching over VCR to CAM		24	0C
1F8	L.LIGHT	LIGHT_ON_MEAN		Mean luminance when LOW LIGHT is ON under normal mode		FF	24
1F9	L.LIGHT	LIGHT_OFF_MEAN		Mean luminance when LOW LIGHT is ON under normal mode		30	30
1FA	L.LIGHT	LIGHT_OFF_GUP		Mean luminance when LOW LIGHT is OFF under gain-up mode		37	37
1FB	BURE	LOW_LIGHT_ON		Threshold for judging blur stopping low luminance (HIGH)		0A	0A
1FC	BURE	SLOW_LIGHT_OFF		Threshold for judging blur stopping low luminance (LOW)		14	14
1FD	L.LIGHT	NOISE_CLIP_START		Low illuminance normal noise clip control start AGC data		70	70
1FE	L.LIGHT	NOISE_CLIP_END		Low illuminance normal noise clip control end AGC data		B6	B6
1FF	L.LIGHT	NOISE_CLIP_MAX		Low illuminance normal noise clip max. value ▲2		3F	3F
200	L.LIGHT	NOISE_CLIP_GUP_MAX		Low illuminance gain-up noise clip max. value		3F	3F
201		ezm_v_offset		▲6		00	00
202		pbzm_v_offset		▲6		00	00
203	L.LIGHT	RESERVE				FF	FF
204		overlap_time		Overlap time		B4	96
205	L.LIGHT	STUP_START		Low-illuminance normal set-up control start AGC data ▲2		70	92
206	L.LIGHT	STUP_END		Low-illuminance normal set-up control end AGC data ▲2		A0	AA
207	L.LIGHT	KSETUP_OFSET		Low-illuminance normal set-up offset value ▲2		03	05
208	L.LIGHT	KSETUP_OFST_GUP		Low-illuminance gain-up set-up offset value		00	00
209	L.LIGHT	CFAD_START		Low-illuminance normal color suppression start AGC data ▲2		66	83
20A	L.LIGHT	CFAD_END		Low-illuminance normal color suppression end AGC data ▲2		A0	AA
20B	L.LIGHT	CFAD_MIN		Low-illuminance normal color suppression min. level		28	2F
20C	L.LIGHT	CFAD_GUP_MIN		Low-illuminance gain-up color suppression min. level		1C	2C
20D	CAM DSP	KSETUP_OFST_SKI		Set-up offset value under skiing mode		FD	FD
20E	CAM DSP	KSYNC_OFST_SKI		Sink level offset value under skiing mode		FE	FE
20F	D/A	YGAIN_OFST_SKI		Y-gain offset value under skiing mode		FD	FD
210	AWB	WB_IREF_OUT		▲5		04	12
211	AWB	WB_QREF_OUT		▲5		02	06
212	AWB	WB_START_I				FE	FE
213	AWB	WB_DIFF_OUT				04	04
214	E_ZOOM	IRSTART_CAM		Still unit start timing under CAM mode ▲4		04	04
215	E_ZOOM	IRSTART_VRT		Still unit start timing under VCR mode ▲4		0C	0C
216	BURE	fad_tst_cam		FAD_TST parameter under CAM mode		20	20
217	BURE	fad_tst_vcr		FAD_TST parameter under VCR mode		60	60

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
218	BURE	X_REACT_THRESH		Threshold for horizontal-direction dead zone		04	04
219	BURE	X_REACT_THRESH		Threshold for vertical-direction dead zone		04	04
21A	BURE	X_EZM_RISE		Increment of horizontal-direction compensation at electronic zooming + blurring		10	10
21B	BURE	X_EZM_RISE		increment of vertical-direction compensation at electronic zooming + blurring		10	10
21C	BURE	MOV_JUDGE_NG		Moving subject rejection threshold		46	46
21D	BURE	MOV_JUDGE_OK		Moving subject acceptation threshold		8A	8A
21E	BURE	MOVE_JUDGE_THRESH		Moving subject judgment threshold		12	12
21F	BURE	TDX		Threshold for horizontal concentration gradient TDX		04	04
220	AWB	TDY		Threshold for vertical concentration gradient TDY		04	04
221	AWB	RLN		Number of blocks for judging TDX, TDY		0E	0E
222	AWB	THDV		Threshold for acceptation/rejection judgment of concentration gradient		02	02
223	AWB	THFD		Threshold for horizontal cumulative function gradient		08	08
224	AWB	THHB		Threshold for vertical cumulative function gradient		08	08
225	AWB	HDTL_L_WIDTH1				14	14
226	BURE	HDTL_L_WIDTH1				14	14
227	BURE	VDTL_WIDTH1				14	14
228	BURE	HDTL_L_WIDTH2				10	10
229	BURE	HDTL_L_WIDTH2				10	10
22A	BURE	VDTL_WIDTH2				10	10
22B	BURE	LOW_LIGHT_DTL				90	90
22C	BURE	HZM_DLY_EZM				12	12
22D	BURE	HZM_DLY_DNR				1B	1B
22E	BURE	TST_V2M1_12				88	88
22F	BURE	TST_V2M1_24				87	87
230	BURE	HPF_KYB				7F	7F
231	BURE	HPF_KYB				7F	7F
232	BURE	LOW_CONT_H				C4	C4
233	BURE	LOW_CONT_L				C0	C0
234	BURE	IR_WEFM2				8C	8C
235	BURE	CBLK_SP_OFFSET				00	00
236	E_ZOOM	hsft_p0_vcr_receive				00	00
237	E_ZOOM	hsft_p1_vcr_receive				09	09
238	E_ZOOM	mv_tst_receive		▲4		84	84
239	E_ZOOM	mv_tst_still		▲4		84	84
23A	E_ZOOM	mv_tst_field		▲4		88	88
23B		RESERVE		Unused		FF	FF
23C		RESERVE		Unused		FF	FF
23D		RESERVE		Unused		FF	FF
23E		RESERVE		Unused		FF	FF
23F		RESERVE		Unused		FF	FF
240		RESERVE		Unused		FF	FF
241		RESERVE		Unused		FF	FF
242		RESERVE		Unused		FF	FF
243		RESERVE		Unused		FF	FF
244		RESERVE		Unused		FF	FF
245		RESERVE		Unused		FF	FF
246		RESERVE		Unused		FF	FF
247		RESERVE		Unused		FF	FF
248		RESERVE		Unused		FF	FF

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
249		RESERVE		Unused		FF	FF
24A		RESERVE		Unused		FF	FF
24B		RESERVE		Unused		FF	FF
24C		RESERVE		Unused		FF	FF
24D		RESERVE		Unused		FF	FF
24E		RESERVE		Unused		FF	FF
24F		RESERVE		Unused		FF	FF
250		RESERVE		Unused		FF	FF
251		RESERVE		Unused		FF	FF
252		RESERVE		Unused		FF	FF
253		RESERVE		Unused		FF	FF
254		RESERVE		Unused		FF	FF
255		RESERVE		Unused		FF	FF
256		RESERVE		Unused		FF	FF
257		RESERVE		Unused		FF	FF
258		RESERVE		Unused		FF	FF
259		RESERVE		Unused		FF	FF
25A		RESERVE		Unused		FF	FF
25B		RESERVE		Unused		FF	FF
25C		RESERVE		Unused		FF	FF
25D		RESERVE		Unused		FF	FF
25E		RESERVE		Unused		FF	FF
25F		RESERVE		Unused		FF	FF
260	E-ZOOM	irhe_st1_cam	2C			75	75
261	E-ZOOM	irhe_ed1_cam	2E			75	75
262	E-ZOOM	irve_st0_cam	2F			00	00
263	E-ZOOM	irve_st1_cam	30			11	29
264	E-ZOOM	irve_ed0_cam	31			01	01
265	E-ZOOM	irve_ed1_cam	32			01	19
266	E-ZOOM	wefmz_ed0_cam	38			03	03
267	E-ZOOM	wefmz_ed1_cam	39			71	71
268	E-ZOOM	wven_st0_cam	3A			00	00
269	E-ZOOM	wven_st1_cam	3B			0F	0F
26A	E-ZOOM	wven_ed0_cam	3C			01	01
26B	E-ZOOM	wven_ed1_cam	3D	▲6		02	32
26C	E-ZOOM	rven_st0_cam	42			00	00
26D	E-ZOOM	rven_st1_cam	43			0E	0E
26E	E-ZOOM	rven_ed0_cam	44			01	01
26F	E-ZOOM	rven_ed1_cam	45	▲6		02	32
270	E-ZOOM	irtmg_cam_send	47	▲5		0F	0F
271	E-ZOOM	refmz_ed1_cam	51			65	65
272	E-ZOOM	henz_ed1_cam	55			65	65
273	E-ZOOM	rst88_pol_cam	5B			34	34
274	E-ZOOM	wefmn_ed1_cam	61			80	80
275	E-ZOOM	refmn_ed1_cam	65			45	45
276	E-ZOOM	henn_ed1_cam	69			61	61
277	E-ZOOM	he0z_ed1_cam	6D			45	45
278	E-ZOOM	he0n_ed1_cam	71			46	46
279	E-ZOOM	cb1k_vcst0_cam	74			00	00

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
27A	E-ZOOM	cb1k_hcst1_cam	75	▲6		10	10
27B	E-ZOOM	cb1k_vced0_cam	76			01	01
27C	E-ZOOM	cb1k_vced1_cam	77	▲6		01	01
27D	E-ZOOM	cb1k_hcst1_cam	79			68	68
27E	E-ZOOM	cb1k_hced1_cam	7B	▲5		FE	FE
27F	E-ZOOM	rst48b_po1_cam	7F			36	36
280	E-ZOOM	rven0_st0_cam	8B			00	00
281	E-ZOOM	rven0_st1_cam	8C			0E	0E
282	E-ZOOM	rven0_ed0_cam	8D			01	01
283	E-ZOOM	rven0_ed1_cam	8E	▲6		02	32
284	E-ZOOM	hsft_p0_cam	8F			00	00
285	E-ZOOM	hsft_p1_cam	90			0A	0A
286	E-ZOOM	shsft_p0_cam	91	▲5		00	03
287	E-ZOOM	shsft_p1_cam	92	▲5		05	8B
288	E-ZOOM	irtng_cam_recv	47	▲5		15	0D
289		RESERVE		Unused		FF	FF
28A		RESERVE		Unused		FF	FF
28B		RESERVE		Unused		FF	FF
28C		RESERVE		Unused		FF	FF
28D		RESERVE		Unused		FF	FF
28E		RESERVE		Unused		FE	FE
28F		RESERVE		Unused		FF	FF
290	E-ZOOM	irhe_st1_vcr	2C	▲6		79	79
291	E-ZOOM	irhe_ed1_vcr	2E	▲6		49	49
292	E-ZOOM	irhe_st0_vcr	2F			00	00
293	E-ZOOM	irhe_st1_vcr	30			15	2D
294	E-ZOOM	irhe_ed0_vcr	31			01	01
295	E-ZOOM	irve_ed1_vcr	32			05	1D
296	E-ZOOM	wefmz_ed0_vcr	38			00	00
297	E-ZOOM	wefmz_ed1_vcr	39			06	06
298	E-ZOOM	wven_st0_vcr	2A			00	00
299	E-ZOOM	wven_st1_vcr	3B			13	13
29A	E-ZOOM	wven_ed0_vcr	3C			01	01
29B	E-ZOOM	wven_ed1_vcr	3D	▲6		06	36
29C	E-ZOOM	rven_st0_vcr	42			00	00
29D	E-ZOOM	rven_st1_vcr	43			12	12
29E	E-ZOOM	rven_ed0_vcr	44			01	01
29F	E-ZOOM	rven_ed1_vcr	45	▲6		06	36
2A0	E-ZOOM	irtmg_vcr_send	47	▲5		13	1B
2A1	E-ZOOM	refmz_ed1_vcr	51			2D	2D
2A2	E-ZOOM	henz_ed1_vcr	55			4C	4C
2A3	E-ZOOM	rst88_po1_vcr	5B			32	32
2A4	E-ZOOM	wefmn_ed1_vcr	61			58	58
2A5	E-ZOOM	refmn_ed1_vcr	65			25	25
2A6	E-ZOOM	henn_ed1_vcr	69			51	51
2A7	E-ZOOM	he0z_ed1_vcr	6D			3E	3E
2A8	E-ZOOM	he0n_ed1_vcr	71			36	36
2A9	E-ZOOM	cblkvvcst0_vcr	74			00	00
2AA	E-ZOOM	cblk_vcst1_vcr	75	▲6		14	14

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
2AB	E-ZOOM	cblk_vced0_vcr	76			01	01
2AC	E-ZOOM	cblk_vced1_vcr	77	▲6		05	05
2AD	E-ZOOM	cblk_hcst1_vcr	79			7D	7D
2AE	E-ZOOM	cblk_hcst0_vcr	78	▲6		44	44
2AF	E-ZOOM	rst48b_po1_vcr	7F			32	32
2B0	E-ZOOM	rven0_st0vsend	8B			00	00
2B1	E-ZOOM	rven0_st1_send	8C			12	12
2B2	E-ZOOM	rven0_ed0_send	8D			01	01
2B3	E-ZOOM	rven0_st1_send	8E	▲6		06	36
2B4	E-ZOOM	hsft_p0_vcr	8F			00	00
2B5	E-ZOOM	hsft_p1_vcr	90			09	09
2B6	E-ZOOM	shsft_p0_vcr	91			00	00
2B7	E-ZOOM	shsft_p1_vcr	92	▲5		09	11
2B8	E-ZOOM	irtmg-rtr-vecv	47	▲3		18	18
2B9		RESERVE		Unused		FF	FF
2BA		RESERVE		Unused		FF	FF
2BB		RESERVE		Unused		FF	FF
2BC		RESERVE		Unused		FF	FF
2BD		RESERVE		Unused		FF	FF
2BE		RESERVE		Unused		FF	FF
2BF		RESERVE		Unused		FF	FF
2C0	E-ZOOM	RESERVE		Unused		FF	FF
2C1	E-ZOOM	EZM-BLKLVL	02	Blanking signal level switch		00	00
2C2	E-ZOOM	EZM-ESUPD	03	Encorder setup level		00	00
2C3	E-ZOOM	RESERVE		Unused		FF	FF
2C4	E-ZOOM	RESERVE		Unused		FF	FF
2C5	E-ZOOM	RESERVE		Unused		FF	FF
2C6	E-ZOOM	EZM_ZREAD	07			00	00
2C7	E-ZOOM	RESERVE		Unused		FF	FF
2C8	E-ZOOM	EZM_THIM	0F			FA	FA
2C9	E-ZOOM	EZM_EMOV	10			34	34
2CA	E-ZOOM	EZM_ESTIL	11			1E	1E
2CB	E-ZOOM	EZM_PDOWN	18			00	00
2CC	E-ZOOM	RESERVE		Unused		FF	FF
2CD	E-ZOOM	RESERVE		Unused		FF	FF
2CE	E-ZOOM	RESERVE		Unused		FF	FF
2CF	E-ZOOM	EZM_HVSEL	1C			10	10
2D0	E-ZOOM	EZM_MTST	1D			00	00
2D1	E-ZOOM	EZM_OUT_SEL	1E			60	60
2D2	E-ZOOM	EZM_OUT_TST0	1F			00	00
2D3	E-ZOOM	EZM_CTL_TST1	20			00	00
2D4	E-ZOOM	EZM_CTL_TST2	21			00	00
2D5	E-ZOOM	EZM_TST_HZM0	22			04	04
2D6	E-ZOOM	EZMVTST_HZM1	23			00	00
2D7	E-ZOOM	EZM_TST_VZM0	24			00	00
2D8	E-ZOOM	EZM_TST_VZM1	25			00	00
2D9	E-ZOOM	EZM_DNR_TST	26			00	00
2DA	E-ZOOM	RESERVE		Unused		FF	FF
2DB	E-ZOOM	RESERVE		Unused		FF	FF

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
2DC	E-ZOOM	RESERVE		Unused		FF	FF
2DD	E-ZOOM	RESERVE		Unused		FF	FF
2DE	E-ZOOM	EZM_IRHE_ST0	2B			00	00
2DF	E-ZOOM	RESERVE		Unused		FF	FF
2E0	E-ZOOM	EZM_IRHEVEDO	2D			03	03
2E1	E-ZOOM	RESERVE		Unused		FF	FF
2E2	E-ZOOM	RESERVE		Unused		FF	FF
2E3	E-ZOOM	RESERVE		Unused		FF	FF
2E4	E-ZOOM	RESERVE		Unused		FF	FF
2E5	E-ZOOM	RESERVE		Unused		FF	FF
2E6	E-ZOOM	EZM_IROSET	33			08	08
2E7	E-ZOOM	EZMVTG_HLP0	34			17	17
2E8	E-ZOOM	EZM_TG_HLP1	35			F7	F7
2E9	E-ZOOM	EZM_WEFMZ_ST0	36			00	00
2EA	E-ZOOM	EZM_WEFMZ_ST1	37			71	71
2EB	E-ZOOM	RESERVE		Unused		FF	FF
2EC	E-ZOOM	RESERVE		Unused		FF	FF
2ED	E-ZOOM	EZM_WVEN_ST0	3A			00	00
2EE	E-ZOOM	EZM_WVEN_ST1	3B			0F	0F
2EF	E-ZOOM	EZM_WVEN_ED0	3C			01	01
2F0	E-ZOOM	EZM_WVEN_ED1	3D			02	02
2F1	E-ZOOM	RESERVE		Unused		FF	FF
2F2	E-ZOOM	RESERVE		Unused		FF	FF
2F3	E-ZOOM	RESERVE		Unused		FF	FF
2F4	E-ZOOM	RESERVE		Unused		FF	FF
2F5	E-ZOOM	RESERVE		Unused		FF	FF
2F6	E-ZOOM	RESERVE		Unused		FF	FF
2F7	E-ZOOM	RESERVE		Unused		FF	FF
2F8	E-ZOOM	RESERVE		Unused		FF	FF
2F9	E-ZOOM	RESERVE		Unused		FF	FF
2FA	E-ZOOM	RESERVE		Unused		FF	FF
2FB	E-ZOOM	EZM_IRHPD	48	▲5		82	82
2FC	E-ZOOM	EZM_IR_REFM	49			00	00
2FD	E-ZOOM	EZM_VDK_VC0	4A			00	00
2FE	E-ZOOM	EZM_VDKVVC1	4B			0A	0A
2FF	E-ZOOM	EZM_VDK_HC0	4C			00	00
300	E-ZOOM	EZM_VDK_HC1	4D			01	01
301	E-ZOOM	EZM_REFMZ_ST0	4E			00	00
302	E-ZOOM	EZM_REFMZ_ST1	4F			45	45
303	E-ZOOM	EZM_REFMZ_ED0	50			03	03
304	E-ZOOM	RESERVE		Unused		FF	FF
305	E-ZOOM	EZM_HENZ_ST0	52			00	00
306	E-ZOOM	EZM_HENZ_ST1	53			65	65
307	E-ZOOM	EZM_HENZ_ED0	54			03	03
308	E-ZOOM	RESERVE		Unused		FF	FF
309	E-ZOOM	RESERVE		Unused		FF	FF
30A	E-ZOOM	EZM_RST48N_P00	57			00	00
30B	E-ZOOM	EZM_RST48N_P01	58			35	35
30C	E-ZOOM	RESERVE		Unused		FF	FF

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
30D	E-ZOOM	EZM_RST88_P00	5A			00	00
30E	E-ZOOM	RESERVE		Unused		FF	FF
30F	E-ZOOM	RESERVE		Unused		FF	FF
310	E-ZOOM	RESERVE		Unused		FF	FF
311	E-ZOOM	EZM_WEFMN_ST0	5E			00	00
312	E-ZOOM	EZM_WEFMN_ST1	5F			80	80
313	E-ZOOM	EZM_WEFMN_ED0	60			03	03
314	E-ZOOM	RESERVE		Unused		FF	FF
315	E-ZOOM	EZM_REFMN_ST0	62			00	00
316	E-ZOOM	EZM_REFMN_ST1	63			45	45
317	E-ZOOM	EZM_REFMN_ED0	64			03	03
318	E-ZOOM	RESERVE		Unused		FF	FF
319	E-ZOOM	EZM_HENN_ST0	66			00	00
31A	E-ZOOM	EZM_HENN_ST1	67			62	62
31B	E-ZOOM	EZM_HENN_ED0	68			03	03
31C	E-ZOOM	RESERVE		Unused		FF	FF
31D	E-ZOOM	EZM_HEOZ_ST0	6A			00	00
31E	E-ZOOM	EZM_HEOZ_ST1	6B			45	45
31F	E-ZOOM	EZM_HEOZ_ED0	6C			03	03
320	E-ZOOM	RESERVE		Unused		FF	FF
321	E-ZOOM	EZM_HEON_ST0	6E			00	00
322	E-ZOOM	EZM_HEON_ST1	6F			46	46
323	E-ZOOM	EZM_HEON_ED0	70			03	03
324	E-ZOOM	RESERVE		Unused		FF	FF
325	E-ZOOM	EZM_TST_SUNT	72			0D	0D
326	E-ZOOM	RESERVE		Unused		FF	FF
327	E-ZOOM	RESERVE		Unused		FF	FF
328	E-ZOOM	RESERVE		Unused		FF	FF
329	E-ZOOM	RESERVE		Unused		FF	FF
32A	E-ZOOM	RESERVE		Unused		FF	FF
32B	E-ZOOM	EZM_CBLK_HCST0	78			00	00
32C	E-ZOOM	RESERVE		Unused		FF	FF
32D	E-ZOOM	EZM_CBLK_HCED0	7A			03	03
32E	E-ZOOM	RESERVE		Unused		FF	FF
32F	E-ZOOM	EZM_RST84_P00	7C			00	00
330	E-ZOOM	EZM_RST84_P01	7D			53	53
331	E-ZOOM	EZM_RST48B_P00	7E			00	00
332	E-ZOOM	RESERVE		Unused		FF	FF
333	E-ZOOM	EZM_TST_ISEL	80			00	00
334	E-ZOOM	EZM_MV_KINY	81			22	22
335	E-ZOOM	EZM_MV_KINC	82			0C	0C
336	E-ZOOM	EZM_MV_THY	83			04	04
337	E-ZOOM	EZM_MV_THC	84			0C	0C
338	E-ZOOM	EZM_MV_PA	85			07	07
339	E-ZOOM	RESERVE		Unused		FF	FF
33A	E-ZOOM	EZM_VT_VTH	87			0C	0C
33B	E-ZOOM	EZM_TST_VT0	88			00	00
33C	E-ZOOM	EZM_TST_VT1	89			00	00
33D	E-ZOOM	EZM_TST_HZM2	8A			00	00

ADRS	PART	LABEL	DSP ADRS	Description	MAX	NTSC	PAL
33E	E-ZOOM	RESERVE		Unused		FF	FF
33F	E-ZOOM	RESERVE		Unused		FF	FF
340	E-ZOOM	RESERVE		Unused		FF	FF
341	E-ZOOM	RESERVE		Unused		FF	FF
342	E-ZOOM	RESERVE		Unused		FF	FF
343	E-ZOOM	RESERVE		Unused		FF	FF
344	E-ZOOM	RESERVE		Unused		FF	FF
345	E-ZOOM	RESERVE		Unused		FF	FF
346	E-ZOOM	EZM_WR_OFFSET	93			04	04
347	E-ZOOM	RESERVE		Unused		FF	FF
348	E-ZOOM	RESERVE		Unused		FF	FF
349	E-ZOOM	RESERVE		Unused		FF	FF
34A	E-ZOOM	RESERVE		Unused		FF	FF
34B	E-ZOOM	RESERVE		Unused		FF	FF
34C	E-ZOOM	RESERVE		Unused		FF	FF
34D	E-ZOOM	RESERVE		Unused		FF	FF
34E	E-ZOOM	RESERVE		Unused		FF	FF
34F	E-ZOOM	RESERVE		Unused		FF	FF
350	E-ZOOM	RESERVE		Unused		FF	FF
351	E-ZOOM	RESERVE		Unused		FF	FF
352	E-ZOOM	RESERVE		Unused		FF	FF
353	E-ZOOM	RESERVE		Unused		FF	FF
354	E-ZOOM	RESERVE		Unused		FF	FF
355	E-ZOOM	RESERVE		Unused		FF	FF
356	E-ZOOM	RESERVE		Unused		FF	FF
357	E-ZOOM	RESERVE		Unused		FF	FF
358	E-ZOOM	RESERVE		Unused		FF	FF
359	E-ZOOM	RESERVE		Unused		FF	FF
35A	E-ZOOM	RESERVE		Unused		FF	FF
35B	E-ZOOM	RESERVE		Unused		FF	FF
35C	E-ZOOM	RESERVE		Unused		FF	FF
35D	E-ZOOM	RESERVE		Unused		FF	FF
35E	E-ZOOM	RESERVE		Unused		FF	FF
35F	E-ZOOM	RESERVE		Unused		FF	FF

9. Terminal assignment DC3 lens microprocessor

No.	Terminal name	Terminal function name	I/O	Description
1	P32/SCK0	CLK	O	DA, shutter Serial clock
2	P33/S00/SB0	DATA	O	DA, shutter Serial data
3	P34/T00	NC [FD CLK]	O [O]	LOW output [H800: Focus motor drive Clock for inclination]
4	P35/T01	FM CTL	O	Focus linear motor drive output ON/OFF (HIGH: Output ON)
5	P36/T02	ZD CLK	O	Zoom motor drive Clock for inclination
6	P37/T03	ZM CLK	O	Zoom motor driver output ON/OFF (HIGH: Output ON)
7	RESET	RES	I	Reset input
8	Vdd	VCC		2.8V power supply (min. 2.7V
9	X2	XTAL	I	16MHz X'tal connection terminal
10	X1	EXTAL	I	16MHz X'tal connection terminal
11	Vss	GND		
12	P00	(NC) [FD 1]	O [O]	LOW output [H800: Focus motor drive 1 (1-2 phase excitation type)]
13	P01	D_C [FD 2]	I [O]	Comparative signal between MR_C and MR_Bk [H800: Focus motor drive 2 (1-2 phase excitation type)]
14	P02	D_B [FD 3]	I [O]	Comparative signal between MR_B and MR_A [H800: Focus motor drive 3 (1-2 phase excitation type)]
15	P03	D_A [FD 4]	I [O]	Comparative signal between MR_A and MR_C [H800: Focus motor drive 4 (1-2 phase excitation type)]
16	P04	ZD1	O	Zoom motor control 1 (2-phase excitation type)
17	P05	ZD2	O	Zoom motor control 2 (2-phase excitation type)
18	P06	NC	O	LOW output
19	P07	NC	O	LOW output
20	P67/REFREQ/HLDAY	HALL BIAS	O	Hole element bias current switch
21	P66/WAIT/HLDRQ	ZM CE	O	Zoom motor driver power control (HIGH: Power ON)
22	P65/WR	SHT STB	O	Shutter control strobe
23	P64/RD	DA STB	O	DA data strobe ("H" ACTIVE)
24	P63/A19	ROM DATA	I/O	E²PROM serial data input/output
25	P62/A18	ROM CLK	O	E²PROM serial clock
26	P61/A17	NC	O	LOW output
27	P60/A16	CDS TG PS	O	CDS/TG power save mode "L: Power save" (VCR mode)
28	P57/A15	TGMR1	O	Connected to MR1 terminal of TG for setting the phase selection of clock
29	P56/A14	TGMR2	O	Connected to MR2 terminal of TG for setting the phase selection of clock
30	P55/A13	TGMC1	O	Connected to MC1 terminal of TG for setting the phase selection of clock
31	P54/A12	TGMC2	O	Connected to MC2 terminal of TG for setting the phase selection of clock
32	P53/A10	TGMS1	O	Connected to MS1 terminal of TG for setting the phase selection of clock
33	P52/A9	TGMS2	O	Connected to MS2 terminal of TG for setting the phase selection of clock
34	P51/A8	TGMF1	O	Connected to MF1 terminal of TG for setting the phase selection of clock
35	P50/A7	TGMF2	O	Connected to MF2 terminal of TG for setting the phase selection of clock
36	P47/AD7	NC	O	LOW output
37	P46/AD6	NC	O	LOW output
38	P45/AD5	NC	O	LOW output
39	P44/AD4	NC	O	LOW output
40	P43/AD3	NC	O	LOW output
41	P42/AD2	NC	O	LOW output
42	P41/AD1	NC	O	LOW output

Function with — is not used. *: During resetting, I/O ports are all at the high impedance.

No.	Terminal name	Terminal function name	I/O	Description
43	P40/~~AD0~~	NC	O	LOW output
44	~~ASTB~~/CLKOUT	NC	O	LOW output
45	Vss	GND		GND
46	TEST	GND		GND
47	~~P10~~/PWM0	FM PWM	O	Focus motor control signal
48	P11/~~PWM1~~	NC	O	LOW output
49	P12/~~ASCK2~~/SCK2	TEST2	O	OSD CLK output (OSD for debug at P50 and P51 is controlled.)
50	P13/RxD2/~~S12~~	TEST1	O	LOW output
51	P14/~~TxD2~~/S02	TEST0	O	OSD DATA output, RS-232C data output
52	P15	TEST3	O	Debug pulse output
53	P16	NC	O	LOW output
54	P17	NC	O	LOW output
55	Vdd	VCC	I	2.8V (min2.7V)
56	~~P70~~/ANI0	MR A [PHIR F]	I [1]	RA sensor A analog input [H800: Focus motor Photo interrupter input]
57	~~P71~~/ANI1	MR B	I	RA sensor B analog input
58	~~P72~~/ANI2	MR C	I	RA sensor C analog input
59	~~P73~~/ANI3	PHIR Z	I	Zoom motor photo interrupter input
60	P74/~~ANI4~~	NC	O	LOW output
61	P75/~~ANI5~~	NC	O	LOW output
62	~~P76~~/ANI16	HALL IN	I	Hole element input
63	P77/~~AN17~~	NC	O	LOW output
64	AVdd	AVCC	I	Analog power supply (Input Vdd or less.)
65	AVrefI	A/D REF	I	A/D reference power supply (AVref1 ≦ AVdd must be satisfied.)
66	AVss	GND		
67	AN00	DEBUG_DA0	O	8-bit debug output 0
68	AN01	DEBUG_DA1	O	8-bit debug output 1
69	AVref2	VCC	O	
70	AVref3	GND	I	
71	P20/~~NM1~~	GND	I	NM1 "L" fixed.
72	~~P21~~/INTP0	VD	I	VD input
73	P22/~~INTP1~~	GND	I	
74	P23/~~INTP2/C1~~	GND	I	
75	~~P24~~/INTP3	READY	I	Serial transfer READY input
76	~~P25/INTP4~~/SCK1	SIO CLK	O	Serial transfer clock output
77	P26/~~INTP5~~	GND	I	
78	P27/~~SI0~~	NTSC/PAL	I	NTSC/PAL selection ("H" PAL "L" NTSC)
79	~~P30/RxD~~/SI1	CAM TO LENS	I	Serial transfer data input
80	~~P31/TxD~~/S01	LENS TO CAM	O	Serial transfer data output

Function with — is not used. *: During resetting, I/O ports are all at the high impedance.

10. E²PROM ADDRESS MAP

◎; Written by micro prossesor of auto ajustment.
●; Written by lens maker.

ADRS	PART	LABEL	Description		MAX	NTSC	PAL	
400	LENS	r_inf_mide_ w	Wide end focus ∞ position	(Upper order)		00	00	◎●
401	LENS			(Lower order)		49	49	◎●
402	LENS	r_inf_tele_ w	Tel. end focus ∞ position	(Upper order)		00	00	◎●
403	LENS			(Lower order)		3C	3C	◎●
404	LENS	r_zoom_lz1_ w	Distance from zoom block pate edge to optical wide end	(Upper order)		00	00	◎●
405	LENS			(Lower order)		85	85	●
406	DEBUG	r_232c_data1_ w	Debug output RAM address 1			FF	FF	●
407	DEBUG					FF	FF	
408	DEBUG	r_232c_data2_ w	Debug output RAM address 2			FF	FF	
409	DEBUG					FF	FF	
40A	DEBUG	r_232c_data3_ w	Debug output RAM address 3			FF	FF	
40B	DEBUG					FF	FF	
40C	DEBUG	r_232c_data4_ w	Debug output RAM address 4			FF	FF	
40D	DEBUG					FF	FF	
40E	DEBUG	r_232c_data5_ w	Debug output RAM address 5			FF	FF	
40F	DEBUG					FF	FF	
410	AF	r_fm_point_ w	Nearly 10 mm linear cut piece			00	00	
411	AF					3F	3F	
412	AF	r_zm_point_ w	Max. zoom position on nearly 10 mm linear line			01	01	
413	AF					77	77	
414	ZOOM	r_zd_clk_ w [0]	Zoom driver clock data 60PPS	(Upper order)		08	09	
415	ZOOM			(Lower order)		23	C4	
416	ZOOM	r_zd_clk_ w [1]	120PPS	(Upper order)		06	07	
417	ZOOM			(Lower order)		82	D0	
418	ZOOM	r_zd_clk_ w [2]	180PPS	(Upper order)		04	05	
419	ZOOM			(Lower order)		57	35	
41A	ZOOM	r_zd_clk_ w [3]	240PPS	(Upper order)		03	03	
41B	ZOOM			(Lower order)		41	E8	
41C	ZOOM	r_zd_clk_ w [4]	300PPS	(Upper order)		02	0031	
41D	ZOOM			(Lower order)		9A	1F	
41E	ZOOM	r_zd_clk_ w [5]	360PPS	(Upper order)		02	02	
41F	ZOOM			(Lower order)		2B	9A	◎
420	AF	r_noise_ hi_min_w	High-band data noise (AGC MIN)	(Upper order)		00	00	◎
421	AF			(Lower order)		FF	FF	◎
422	AF	r_noise_ hi_mid_w	High-band data noise (AGC MAN)	(Upper order)		00	00	◎
423	AF			(Lower order)		FF	FF	◎
424	AF	r_noise_ hi_max_w	High-band data noise (AGC GAIN UP)	(Upper order)		00	00	◎
425	AF			(Lower order)		FF	FF	◎
426	AF	r_noise_ lo_min_w	Low-band data noise (AGC MIN)	(Upper order)		00	00	◎
427	AF			(Lower order)		FF	FF	◎
428	AF	r_noise_ lo_mid_w	Low-band data noise (AGC MAN)	(Upper order)		00	00	◎
429	AF			(Lower order)		FF	FF	◎
42A	AF	r_noise_ lo_max_w	Low-band data noise (AGC GAIN UP)	(Upper order)		00	00	◎
42B	AF			(Lower order)		FF	FF	
42C	SERVO	r_servo_ gain_afmf_w	FAR (for AF/MF)	(Upper order)		02	02	
42D	SERVO			(Lower order)		00	00	

ADRS	PART	LABEL	Description	MAX	NTSC	PAL	
42E	SERVO	r_servo_gain_ zoom_w	NEAR (for zoom) (Upper order)		00	00	
42F	SERVO		(Lower order)		A0	A0	
430	SERVO	r_servo_err_ lmt_eep_w	Servo error limiter (Upper order)		01	01	
431	SERVO		(Lower order)		80	80	
432	SERVO	r_integral_gain_ eep_w	Integral gain NEAR (Upper order)		00	00	
433	SERVO		(Lower order)		1A	1A	◎
434	SERVO	r_pwm_center_w	PWM output center value (Upper order)		07	07	◎
435	SERVO		(Lower order)		FF	FF	
436	AF	r_lpwcon_offset_w	Noise offset for low contrast process		00	00	
437	AF				00	00	
438	INT	r_serial_wait_ a_w	Serial transfer timeover setting value (block A)		01	01	
439	INT				00	00	
43A	INT	r_serial_wait_ b_w	Serial transfer timeover setting value (block B)		07	07	
43B	INT				00	00	
43C	INT	r_vd_wait_ w	Waiting time from VD to lost real time output (Upper order)		02	02	
43D	INT		(Lower order)		90	90	
43E		r_reserve_03e_ w			FF	FF	
43F					FF	FF	
440	LENS	r_inf_search_ far	Fine adjustment search width on FAR side during INF adjustment ▲3		25	25	
441	LENS	r_inf_search_ nesr	Fine adjustment search width on NEAR side during INF adjustment		30	30	
442	LENS	r_inf_search_ far00	Coarse adjustment search width on FAR side during INF adjustment		32	32	
443	LENS	r_inf_search_ near00	Coarse adjustment search width onNEAR side during INF adjustment		32	32	
444	LENS	r_zm_off_ cnt	Waiting time for zoom stepping motor power OFF		02	02	
445	LENS	r_zm_compe_ eep	Zoom hysteresis compensation amount waiting time		00	00	
446	AF	r_noise_gain_ hi	Narrow-band noise level conversion coefficient ▲5		D0	D0	
447	AF	r_noise_gain_ lo	Wide-band noise level conversion coefficient		33	33	
448	AF	r_af_ver0_ eep	Plug 0 for AF operation type switch		FF	FF	
449	AF	r_af_ver1_ eep	Plug 1for AF operation type switch		FF	FF	
44A	AF	r_af_ver2_ eep	Plug 2for AF operation type switch		B3	B3	
44B	AF	r_af_ver3_ eep	Plug 3 for AF operation type switch		38	38	
44C	AF	r_af_ver4_ eep	Plug 4 for AF operation type switch ▲3		8F	8F	
44D	AF	r_af_ver5_ eep	Plug 5 for AF operation type switch		EE	EE	
44E	AF	r_af_ver6_ eep	Plug 6 for AF operation type switch ▲2		BF	BE	
44F	AF	r_af_ver7_ eep	Plug 7 for AF operation type switch		BE	BE	
450	AF	r_af_ speed1	AF inclination speed 1 ▲2		0D	0D	
451	AF	r_af_ speed2	AF inclination speed 2 ▲2		06	06	
452	AF	r_af_ speed3	Max. speed during low control		08	08	
453	AF	r_iris_thresh_ eep	Iris variation check threshold value ▲2		07	07	
454	AF	r_boke_ lcon	Narrow band/wide band difference for fade discrimination		A0	A0	
455	LENS	r_zm_ speed_edge	Zoom speed for detection of zoom initialization edge		03	03	
456	AF	r_up_ down_lvl	Leading-/trailing-edge detection level		02	02	
457	AF	r_boke_ small_level	Judgment value with narrow band ÷ wide band		25	25	
458	AF	r_boke_ large_level	Judgment threshold value with narrow band ÷ wide band ▲5		00	00	
459	AF	r_sky_ ck_dat	Sky judgment threshold value		80	80	
45A	AF	r_100k_ dw_diff1	Judgment value for slow trailing of wide band data		08	08	
45B	AF	r_100k_ dw_diff2	Judgment value for smooth trailing of wide band data		01	01	
45C	AF	r_100k_ lsam_ck_lvl	Judgment rate value for runaway of wide band data		08	08	
45D	AF	r_boke_ avoide	Leading edge threshold value for runaway of wide band data		40	40	

ADRS	PART	LABEL	Description	MAX	NTSC	PAL	
45E	AF	r_over_ inf	Number of over - near ∞ steps		24	24	
45F	AF	r_over_near	Number of over - near steps		FF	FF	
460	AF	r_inf_hosei [0]	Zoom position Infinitive far curve compensation value of 0 - 100		FF	FF	
461	AF	r_inf_hosei [1]	101- 200		FF	FF	
462	AF	r_inf_hosei [2]	201- 300		FF	FF	
463	AF	r_inf_hosei [3]	301- 400		FF	FF	
464	AF	r_inf_hosei [4]	401- 450		FF	FF	
465	AF	r_inf_hosei [5]	451- 500		FF	FF	
466	AF	r_inf_hosei [6]	501- 534		FF	FF	
467	AF	r_inf_hosei [7]	535- 567		FF	FF	
468	AF	r_inf_hosei [8]	568- 600		FF	FF	
469	AF	r_inf_hosei [9]	601- 625		FF	FF	
46A	AF	r_inf_hosei [10]	626- 650		FF	FF	
46B	AF	r_inf_hosei [11]	651 - 674		FF	FF	
46C	AF	r_fm_posi_ rate	∞ - 1 m ratio during leading edge in the signal system adjustment mode		FF	FF	
46D	SERVO	r_servo_torque_ weight	Linear motor torque compensation		04	04	
46E	SERVO	r_pwm_bias_ thresh	Auto bias threshold value of PWM output		FF	FF	
46F	SERVO	r_pwm_bias_ max	Maximum value of PWM auto bias		80	80	
470	SERVO	r_line_posi_ eep	Offset during initialization at the far end		04	04	
471	AF	r_af_spd_ thresh1	Threshold value which uses AF_speed 1 at the level 1		10	10	
472	AF	r_af_spd_ thresh2	Threshold value which sets 2 for AF speed at the level 1		0D	0D	
473	AF	r_af_spd_ thresh3	Threshold value which sets 1 for AF speed at the level 1 ▲6		0C	0C	
474	AF	r_wob_step1	Wobbling step for excessive fade ▲2		04	04	
475	AF	r_wob_step2	Wobbling step except excessive fade ▲2		03	03	
476	AF	r_100k_lsam_eep	Data runaway threshold value		08	08	
477	AF	r_datmns_eep	Reinforced threshold value for judgment of slow trailing		50	50	
478	AF	r_trap_exit_eep	Threshold value for escape from slow focusing		0F	0F	
479	AF	r_at_iris_eep	Iris judgment threshold value at AF		D0	D0	
47A	AF	r_datalm_eep	Panning judgment threshold value of data runaway		0D	0D	
47B	AF	r_fldns_eep	Waiting time until an object becomes stable		00	00	
47C	AF	r_panning_stop_eep	AF stop parameter for panning		03	03	
47D	AF	r_adj_wait_eep	Waiting time for data collection after variation of AGC		20	20	
47E	ZOOM	r_sadj_zm_posi	Zoom position in the adjustment mode of signal system		FF	FF	
47F	ZOOM	r_zm_error	Number of zoom motor step errors		00	00	
480	AF	r_noise_gain_wide	Compensation coefficient of wide angle noise data		05	05	
481	AF	r_wob_max	Max. value of wobbling times		02	02	
482	AF	r_af_ speed4	Focus speed limit value for low illuminance		03	03	
483	SERVO	r_servo_err_lmt_af	Servo error value limiter for AF		12	12	
484	RVO	r_servo_err_lmt_wob	Servo error value limiter for wobbling		12	12	
485	RVO	r_mr_offset_max	Limit of MR magnitude detection		38	38	
486	ZOOM	r_zm_speed_sel	Zoom speed selection		06	06	
487	ZOOM	r_vd_ wait_eep	Waiting time for back-up command		FF	FF	
488	TG	r_tg_clk	TG clock phase switch ▲2		EB	EB	
489	AGC	r_agc_min	AGC minimum value ▲3		33	33	
48A	AGC	r_agc_max	D/A output value for max. AGC ▲3		A0	A0	
48B	AGC	r_gain_up_max	Maximum value of added amount value (upper 8 bits) of gain up mode ▲3		26	26	

ADRS	PART	LABEL	Description	MAX	NTSC	PAL	
48C	ADJ	r_lens_adj_ck	Lens adjustment end check		FF	FF	
48D	DEBUG	r_rs232c_select	Debug output selection		FF	FF	
48E	DEBUG	r_bps_parm	OSD/RS-232C baud rate switch		1F	1F	
48F		r_reserve_8I			FF	FF	
490	LENS	r_lens_version	Lens version		FF	FF	●
491	LENS	r_year	Manufacture year		FF	FF	●
492	LENS	r_month	Manufacture month		FF	FF	●
493	LENS	r_day	Manufacture day		FF	FF	●
494	LENS	r_zoom_xn1	Photo interrupter output A/D value of zoom block plate edge -1		80	80	●
495	LENS	r_zoom_xn2	Photo interrupter output A/D value of zoom block plate edge position		80	80	●
496	LENS	r_zoom_xn3	Photo interrupter output A/D value of zoom block plate edge +1		80	80	●
497	LENS	r_reserve_097			FF	FF	
498	LENS	r_reserve_098			FF	FF	
499	LENS	r_adj_data0	Measurement data 0 during lens adjustment		FF	FF	●
49A	LENS	r_adj_data1	Measurement data 1 during lens adjustment		FF	FF	●
49B	LENS	r_adj_data2	Measurement data 2 during lens adjustment		FF	FF	●
49C	LENS	r_adj_data3	Measurement data 3 during lens adjustment		FF	FF	●
49D	LENS	r_adj_data4	Measurement data 4 during lens adjustment		FF	FF	●
49E	LENS	r_adj_data5	Measurement data 5 during lens adjustment		FF	FF	●
49F	IRIS	r_iris_close	D/A output value during iris closing. (Adjustment data)		90	90	◎●
4A0	IRIS	r_adj_close	Iris closing adjustment parameter		08	08	
4A1	IRIS	r_adj_ hall	Hole offset adjustment starting position. (D/A output value)		90	90	
4A2	IRIS	r_adj_hall_ lmt_l	Hole offset adjustment limiting value. (Hole output A/D voltage value)		C0	C0	
4A3	IRIS	r_adj_hall_ lmt_h	Hole offset adjustment limiting value. (Hole output A/D voltage value)		C8	C8	
4A4	IRIS	r_adj_iris	Iris offset adjustment starting position(Adjustment data)		18	18	
4A5	IRIS	r_adj_iris_lmt_l	Iris offset adjustment starting position(Hole output A/D voltage value)		0C	0C	
4A6	IRIS	r_adj_iris_lmt_h	Iris offset adjustment starting position(Hole output A/D voltage value)		04	04	
4A7	IRIS	r_adj_close_lmt	Closing adjustment limiting value(Hole output A/D voltage value)		6D	6D	
4A8	IRIS	r_adj_iris_dah	D/A output starting position during iris closing adjustment		FA	FA	
4A9	IRIS	r_ae_test1	Hole output A/D value for full opening during hole offset adjustment		C6	C6	
4AA	IRIS	r_hall_bias	Hole bias switch		00	00	◎
4AB	AF	r_tell_pk_eep	Initial value of TELE focusing position		20	20	
4AC	AF	r_dauto_afsx	Initial value of TELE focusing position		01	01	
4AD	AF	r_flat_boke_eep	Noise level conversion switch		08	08	
4AE	AF	r_trap_cnt_eep	Counter for escape from AF level 2		10	10	
4AF	AF	r_af_root_eep	AF restart direction threshold value		32	32	
4B0	AF	r_datmns_cnt_eep	Slow descent judgment enforced threshold value		08	08	
4B1	AF	r_afdata_shift	AF data effective digit selection		01	01	
4B2	AF	r_lvdata_shift	1VD raw rata effective digit selection	▲1	01	01	
4B3	AF	r_spot_hw_start	AF sampling area narrow angle horizontal start address	▲1	2A	2A	
4B4	AF	r_spot_hw_size	Horizontal width	▲1	54	54	
4B5	AF	r_spot_vw_start	AF sampling area narrow angle vertical start address	▲1	38	38	
4B6	AF	r_spot_vw_size	Vertical width	▲1	70	70	
4B7	AF	r_wide_ hw_start	AF sampling area wide angle horizontal start address	▲1	15	15	
4B8	AF	r_wide_ hw_size	Horizontal width	▲1	7E	7E	
4B9	AF	r_wide_ vw_start	AF sampling area wide angle vertical start address	▲1	1C	1C	
4BA	AF	r_wide_ vw_size	Vertical width	▲1	A8	C0	
4BB	AF	r_dir_ cnt_eep	Up/down judgment enable level after inverting	▲1	01	01	

ADRS	PART	LABEL	Description	MAX	NTSC	PAL	
4BC	AF	r_100k_thresh	Wide band data varying rate during restart ▲2		04	04	
4BD	AF	r_zmaf_set	AF operation switch during zooming ▲3		00	00	
4BE	AF	r_zmaf_compe_eep	AF position compensation amount during zooming ▲3		02	02	
4BF	AF	r_zmaf_wob_eep	AF operation wobbling amount during zooming ▲3		02	02	
4C0	AF	r_spd_dwn_eep	AF speed limit threshold value at level 1 ▲3		50	50	
4C1	AF	r_af_speed5	AF lowest speed at level 1 ▲5		02	02	
4C2	AF	r_datmns_ave_eep	Judgment threshold value for slow trailing edge ▲6		04	04	
4C3	AF	r_speed_zm_select	Speed switch according to zoom position ▲6		02	02	
4C4	AF	r_zm_speed_eep	Speed calculation offset according to zoom position ▲6		02	02	
4C5		r_reserve_0c5			FF	FF	
4C6		r_reserve_0c6			FF	FF	
4C7		r_reserve_0c7			FF	FF	
4C8		r_reserve_0c8			FF	FF	
4C9		r_reserve_0c9			FF	FF	
4CA		r_reserve_0ca			FF	FF	
4CB		r_reserve_0cb			FF	FF	
4CC		r_reserve_0cc			FF	FF	
4CD		r_reserve_0cd			FF	FF	
4CE		r_reserve_0ce			FF	FF	
4CF		r_reserve_0cf			FF	FF	
4D0		r_reserve_0d0			FF	FF	
4D1		r_reserve_0d1			FF	FF	
4D2		r_reserve_0d2			FF	FF	
4D3		r_reserve_0d3			FF	FF	
4D4		r_reserve_0d4			FF	FF	
4D5		r_reserve_0d5			FF	FF	
4D6		r_reserve_0d6			FF	FF	
4D7		r_reserve_0d7			FF	FF	
4D8		r_reserve_0d8			FF	FF	
4D9		r_reserve_0d9			FF	FF	
4DA		r_reserve_0da			FF	FF	
4DB		r_reserve_0db			FF	FF	
4DC		r_reserve_0dc			FF	FF	
4DD		r_reserve_0dd			FF	FF	
4DE		r_reserve_0de			FF	FF	
4DF		r_reserve_0df			FF	FF	
4E0		r_reserve_0e0			FF	FF	
4E1		r_reserve_0e1			FF	FF	
4E2		r_reserve_0e2			FF	FF	
4E3		r_reserve_0e3			FF	FF	
4E4		r_reserve_0e4			FF	FF	
4E5		r_reserve_0e5			FF	FF	
4E6		r_reserve_0e6			FF	FF	
4E7		r_reserve_0e7			FF	FF	
4E8		r_reserve_0e8			FF	FF	
4E9		r_reserve_0e9			FF	FF	
4EA		r_reserve_0ea			FF	FF	
4EB		r_reserve_0eb			FF	FF	
4EC		r_reserve_0ec			FF	FF	

ADRS	PART	LABEL	Description	MAX	NTSC	PAL	
4ED		r_reserve_0ed			FF	FF	
4EE		r_reserve_0ee			FF	FF	
4EF		r_reserve_0ef			FF	FF	
4F0	D/A	r_iris_h	ME mode iris control output (upper order) ▲4		00	00	
4F1	D/A	r_iris_l	ME mode iris control output(Lower order) ▲4		00	00	
4F2	D/A	r_iris_offset	Iris offset adjustment value		3B	3B	◎
4F3	D/A	r_hall_offset	Hole offset adjustment value		68	68	◎
4F4	D/A	r_agc_kh	ME mode AGC control output (upper order)		00	00	
4F5	D/A	r_agc_kl	ME mode AGC control output (lower order)		00	00	
4F6	D/A	r_ad_ref	OB clamp level manual adjustment value		30	30	
4F7	D/A	r_da_08	Unused		FF	FF	
4F8	D/A	r_da_09	Unused		FF	FF	
4F9	D/A	r_da_10	Unused		FF	FF	
4FA	D/A	r_da_11	Unused		FF	FF	
4FB	D/A	r_da_12	Unused		FF	FF	
4FC	MICON	r_mode_sel	Mode switch ▲3		FF	FF	
4FD	ADJ	r_afae_adj	Adjustment mode indication		FF	FF	
4FE	ADJ	r_adj_mode	Adjustment mode switch		FF	FF	
4FF	MOCON	r_rom_version	Microcomputer version		FF	FF	

5. DIGITAL OUTPUT

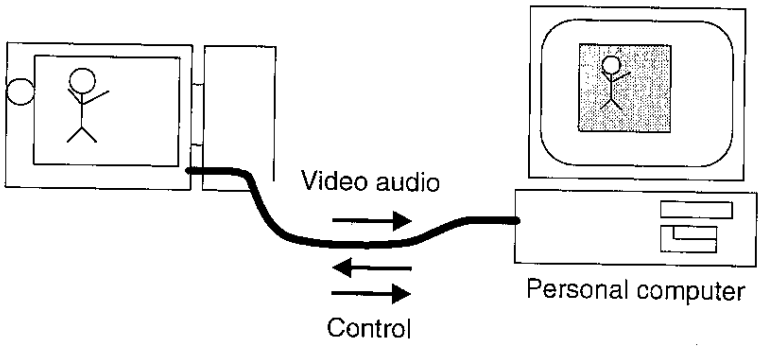
1. Introduction of IEEE1394 digital interface

What is IEEE 1394 digital interface?

IEEE is the abbreviation of THE INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS, and IEEE1394 is on of the serial buses specified and standardized by the institute.

The specifications feature the high speed (100, 200, 400 Mbps) applicable for multimedia, real time transfer, simplified cable, connector, Hot_Plug_In, flexible network structure and so on.

The serial bus uses two sets (data and strobe) of the twist pair signal lines for operation. Since there are two sets alone, the half-duplex mode (bi-directional mode by selecting one-way direction transfer) is applied.On the bus, the video and audio data flows together with the control commands and other control data. Here, the transfer rate of video audio data of DVC approximates 30 Mbps.



2. Circuit configuration and function

Digital interface section

On DC3, IX-0506TAZZ (IC7402) as IEEE1394 exclusive communication control chip and IX-0587TA (IC7401) as the control microprocessor are newly added as the digital interface block. <Refer to the appended drawing.>

IX0506TA is internally divided into the following major sections: (1) Communication section, (2) Video audio data memory control, (3) Command system data memory control section, (4) Data conversion section, and (5) PLL section.

The communication section composes two sets of operation input/output with four terminals, TPA, TPA- and TPB, TPB-. Though IX-0506TA is designed to use a maximum of two ports, one port alone is used on DC3. The end terminal must be properly applied at the port 0 even though it is not used.

PLL uses 8.192MHz of X'tal as the reference, and generates 100MHz (98.3MHz as accurate) necessary for communication and 24MHz as the IC inner operation CLK.

The video audio data is communicated across the transport IC. On the bus 1394, the data are flowed as the data of the synchronous type format. (Isochronous communication)

The data of the command system is communicated across the control microprocessor. (Asynchronous communication)

3. Operation content

When DC3 is powered, IX0506TA in the initialization mode is in the sleep mode in which most of the inner functions are stopped. If the 4-pin cable of DV is connected and 1394IC on the mating side is active, the voltage of TPB terminal of IX0506TA becomes approx. 1.8V. When it detects the rise of the voltage, the control microprocessor judges that it is connected, and resets the sleep mode of IX0506TA to ready the communication.

If any video audio data is then present for output when DC3 is in the PB mode, the microprocessor will operate and output the data for the transport and 1394IC when the bus 1394 is proper.

Since any voltage is not output to TPBISA in the sleep mode, it is supplied from the external buffer. (Otherwise, the sleep mode of the connected mate will be reset.)

The data of the control system is communicated across 1394 IC and microcomputer. If the bus is proper, the data will be flowed regardless of the mode of DC3. However, whether DC3 can be executed for the received command or not is naturally dependent on the operational states.

The video audio data is received across the transport and 1394 IC like the sending (though it is not supported on DC3). Differing from the sending, the frame lock PLL is operated with CLKGEN in order to operate the system synchronously with the received frame pulse.

4. Others

Chip ID

The unit (chip) provided with the communication function of the standard 1394 must have the respectively unique ID (like the global manufacture No.), and it is also written on DC3 during production.If any board (head amplifier board on DC3) with E^2PROM or ROM on which ID is written is replaced during repair, it is necessary to newly write the ID since it is not written.

To obtain ID of IEEE 1394, please correspond to see notify of No. xxx

Here, whether ID is referred to during communication or not is different depending on the application.

5. Cables

Two kinds are approved for the cable and connector of 1394.

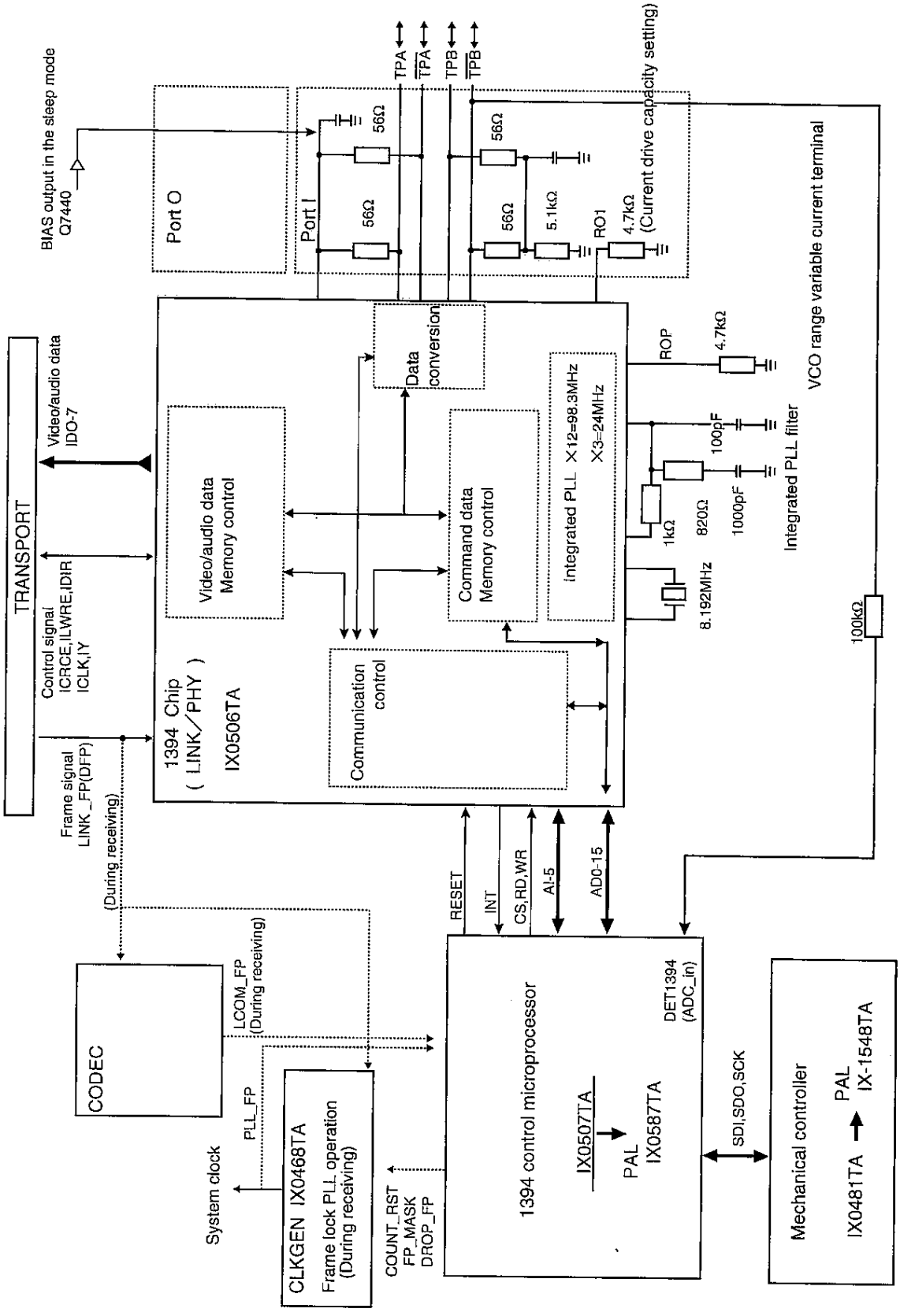
One kind is the 4-pin type (called DV cable/connector) which is used in the DVC instrument, being specified to think much of compactness and flexibility for handling. The cable is specially used for communication of 100 Mbps.

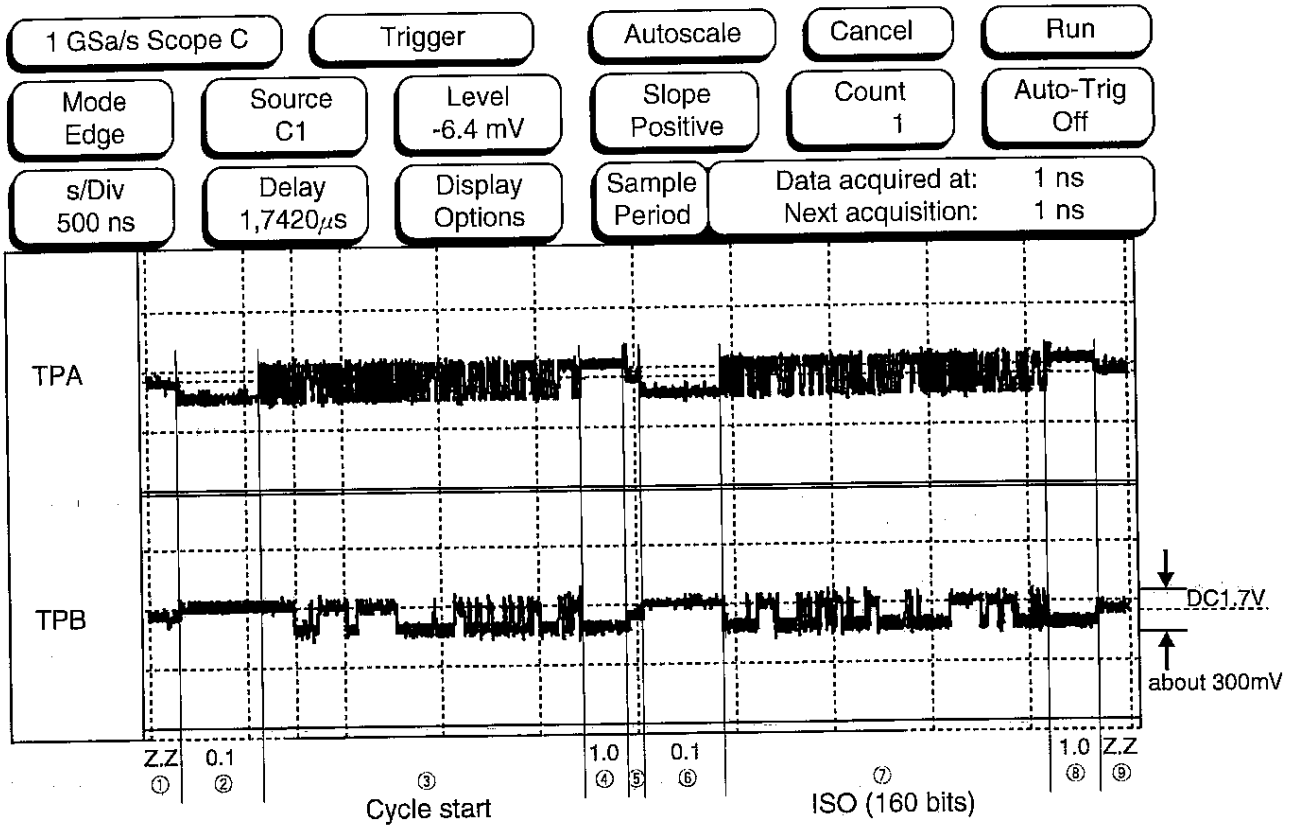
The other kind is the 6-pin type, being possibly adopted mainly as the general purpose port of others except the small portable instruments.

Since the 4-pin type and 6-pin type are not interchangeable with each other, they can not be directly connected. (The converter is necessary.)

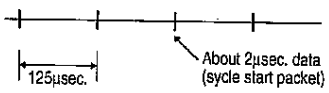
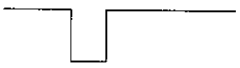
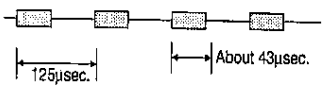
As the signal content, the 4-pin type is produced by eliminating the power supply (VR, VG lines) from the 6-pin type.

■Digital interface block

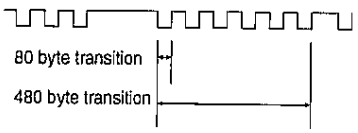



1 GSa/s Scope C
Trigger
Autoscale
Cancel
Run
Mode
Edge
Source
C1
Level
-6.4 mV
Slope
Positive
Count
1
Auto-Trig
Off
s/Div
500 ns
Delay
1,7420μs
Display
Options
Sample
Period
Data acquired at: 1 ns
Next acquisition: 1 ns
TPA
TPB
DC1.7V
about 300mV
Z.Z
①
0.1
②
③
Cycle start
1.0
④
⑤
0.1
⑥
⑦
ISO (160 bits)
1.0
⑧
Z.Z
⑨

3. State transition

Product state	TRANSPORT	Communication IC	Bus 1394
q Power ON	ICLK (9 MHz) output	IC_RESET Sleep	TPA : Bias supply (approx.1.8V) from Q7440 TPB : 0V
w DV_connection		TPB terminal voltage up (1.2V) or more Sleep release Iniciarice Bus 1394	TPB : Bias supply (approx. 1.8V) from TPA of the connected unit When the sleep mode is released TPA: Start of bias supply (approx. 1.8V) from TPBIAS terminal Q7440 is turned off.
e STOP mode	IDIR = 'H' output (ISO sending/receiving Direction setting) IV = 'H' output (Data_Enable_signal: L_Active)	ISO cycle start	It is divided every 125msec. (It means that it is readied to flow ISO_Data.) 
r PB mode	IDIR = 'L' (sending) IV = Varying output of HL (approx. 56KHz) DFP = Frame pulse output (L term is short. Several µsec? or less)	ISO data transition ILWRE = 'L' output (ISO_Data imputable) IV is set at "L" six times.  Data of 80 bytes is input into the communication IC.	ISO_Data is output every 125 µsec. However, ISO_data is omitted at a rate of once per 6 or 7 times.  Frame pulse enters the time stamp into the data. aThe receiving side returns it to its original state.

*IV



*ICRCE : Communication IC output terminal. 'L' stands if CRC error occurs in the ISO_data during sending. Not used during sending.

6. POWER SUPPLY CIRCUIT

VL-DC3 Power circuit control

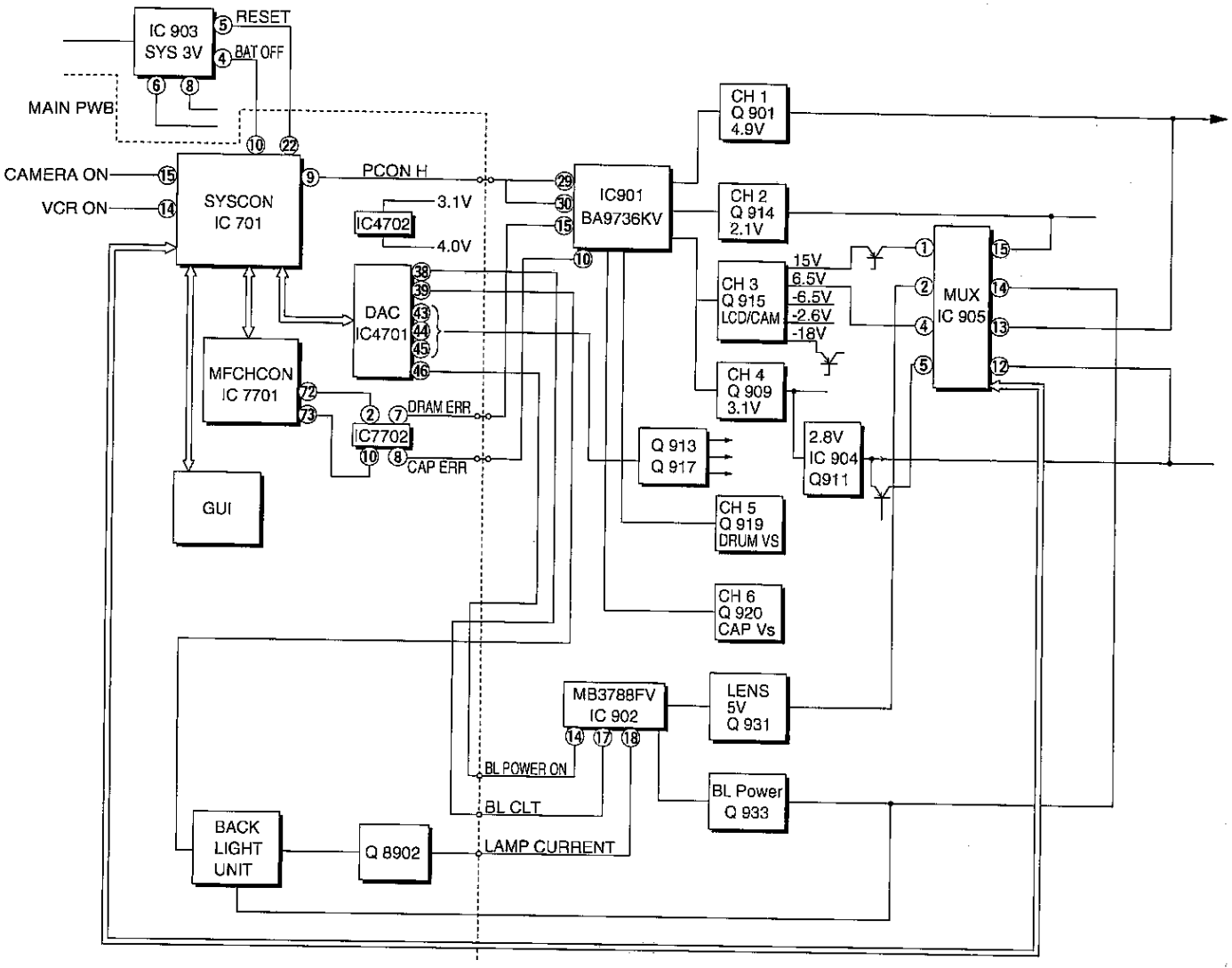
1. Multiplexer control signal

Input data signal			Multiplexer output (POWER CK)	
A	B	C		
0	0	0	x0	P CON 4.9V
1	0	0	x1	BL PWR
0	1	0	x2	D 2.1V
0	1	1	x3	P CON 2.8V
0	0	1	x4	CAM 15V
1	0	1	x5	CAM 2.8V
0	1	1	x6	LENS 5V
1	1	1	x7	LCD 6.5V

2. External switch control signal

Signal name	Terminal	Output
P-CON-H	SYS ⑨	P-CON 4.9V
		D 2.1V
		LCD 6.5V
		P-CON 3.1V(P-CON 2.8V)
		LENS 5V
CAM 15V P-CON	DAC 43	CAM 15V
		CAM –18V
CAM 4.9V P-CON	DAC 44	CAM 4.9V
CAM 2.8V P-CON	DAC 45	CAM 2.8V
BL PWR	DAC 46	BL PWR

■VL-DC3 Series Block diagram

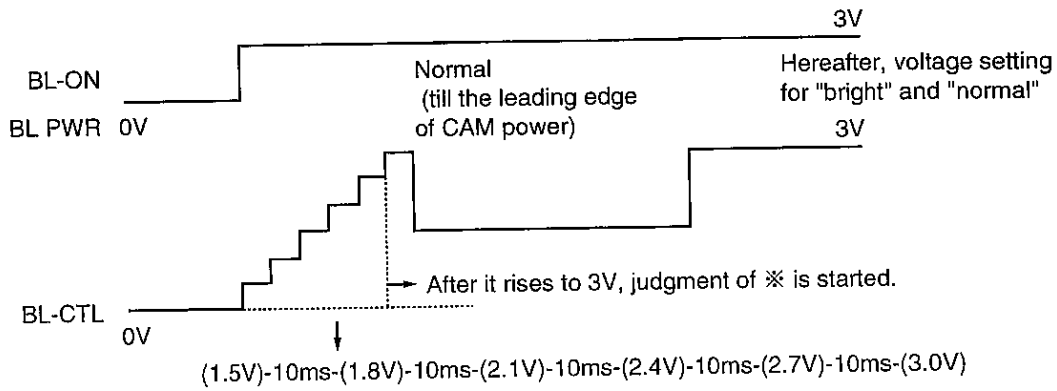


3. Process for leading edge of power supply

Sequence	Multiplexer input terminal	Input power supply line	Judgment conditions	Signaling process for satisfaction of judgs ment condition
①				•P CON H H
②	x0 x2 x3 x6 x7	P - CON 4.9V D 2.1V P-CON 2.8V LENS 5V LCD 6.5V	1.1V or more AND 1.1V or more AND 1.1V or more AND 1.1V or more AND 1.1V or more	• BL-ON, BL PWR H ➡10ms ➡ • BL-CTL
③	x1	BL-PWR	0.875V ~ 2.03V	
④				•CAM 2.8V P-CON H •CAM 4.9V P-CON H •CAM 15V P-CON H
⑤	x4 x5	CAM 15V CAM 2.8V	1.1V or more 1.1V or more	<Leading edge of CAM is completed.>
⑥				•CAM 2.8V P-CON L •CAM 4.9V P-CON L •CAM 15V P-CON L
⑦	x4 x5	CAM 15V CAM 2.8V	1.1V or more 1.1V or less	<Leading edge of VCR is completed.>

- If the voltage does not satisfy the judgment conditions within 100 ms, it will be regarded as a fault to turn the voltage line from the leading edge to the trailing edge.

- Timing relationship among BL-ON, BL PWR and BL-CTL



4. Process for trailing edge of voltage

Sequence	Multiplexer input terminal	Input power supply line	Judgment conditions	Signaling process for satisfaction of judgs ment condition
①				• CAM15V P-CON
②	x4	CAM 15V	1.1V or less	• CAM 2.8V P-CON ➡10ms ➡ • CAM 4.9V P-CON
③	x5	CAM 2.8V	1.1V or less	<Trailing edge of CAM is completed.> •BL PWR •BL-ON •BL-CTL (at the same time)
④	x2	BL-PWR	0.875 or less 2.03 or more	•P-CON-H
⑤	x0 x2 x3 x6 x7	P-CON 4.9V D 2.1V P-CON 3.1V LENS 5V LCD 6.5V	1.1V or less AND 1.1V or less AND 1.1V or less AND 1.1V or less AND 1.1V or less	<Trailing edge of VCR is completed.>

● If the voltage does not satisfy the judgment conditions within 100 ms, the voltage line will be turned to the trailing edge.(P-COM will be all turned off.)

5. Main power controll IC (VHi BA 9736kv -1*)

Structure Silicon monolithic integrated circuit

Product name 6-CH switching regulator controller

Model name BA9736KV

Outline view Fig. 1 (Plastic mold)

Terminal layout Fig. 2

Block diagram Fig. 3

Function

1. The triangular wave oscillator, reference voltage, air lamp, PWM comparator, totempole driver and various protective circuits necessary to compose the switching regulator are integrated in one chip, being a 6-channel control IC specially suitable for movie.
2. The totempole driver can directly drive the power transistor to set ON current at the constant current with the external resistor.
3. The malfunction-protective circuit for low-voltage input is integrated.
4. The output cutoff circuit (timer latch type) for overload pressure is integrated.
5. The totempole driver which rectifies synchronously with the chopper using FET at CH1 and CH4 is integrated. The duty offset with the chopper can be externally adjusted.
6. The channel control turns off all channels when STB is low and turns off the CH3 alone when STB3 is low.
7. The soft start can be controlled with the external capacitor common for all channels and is synchronous with the leading edge of STB and STB3.
8. The package is installed at VQFP-64 (0.5 mm pitch).

■Absolute maximum rating

(Ta = 25°C)

Item	Code	Rating	Unit
Applied voltage	V_{CC}	13.5	V
Output current	I OUT	100	mA
Allowable loss	P_D	(*1) 750	mW
		(*2)1000	mW
Operational temperature range	T_{OP}	–25 ~ +85	°C
Storage temperature range	Tstg	–25 ~ +85	°C

(*1) It decreases 7.5 mW per rise of 1°C of the unit. (25°C or more)
(*2) When 70*70*1.5t PWB is installed.

(VHi MB 3788 FV-1*)

■Max. rating

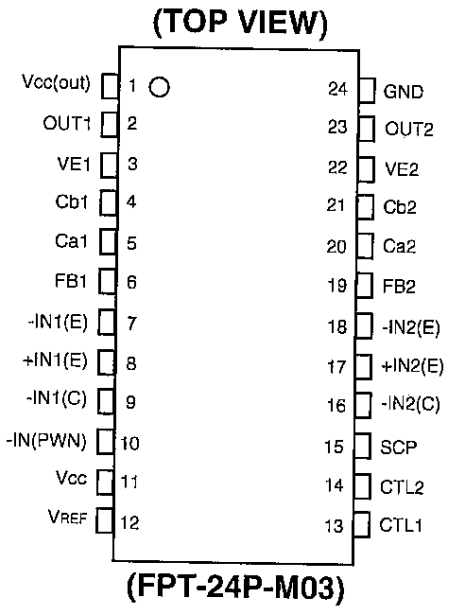
(Ta = +25°C)

Item	Code	Conditions	Rated value	Unit
Power voltage	V_{CC}	–	20	V
Control input voltage	V_{ICTL}	–	20	V
Tolerable loss	P_D	Ta ≦ + 25℃	500*	mW
Operational environmental temperature	T_{OP}	–	–30~+85	℃
Storage temperature	Tstg	–	–55~+125	℃

* The data are applicable if it is installed on 4 cm square both-side epoxy board.
Soldering temperature/time: 260℃/10 seconds

6. Performance specifications

■Terminal assignment

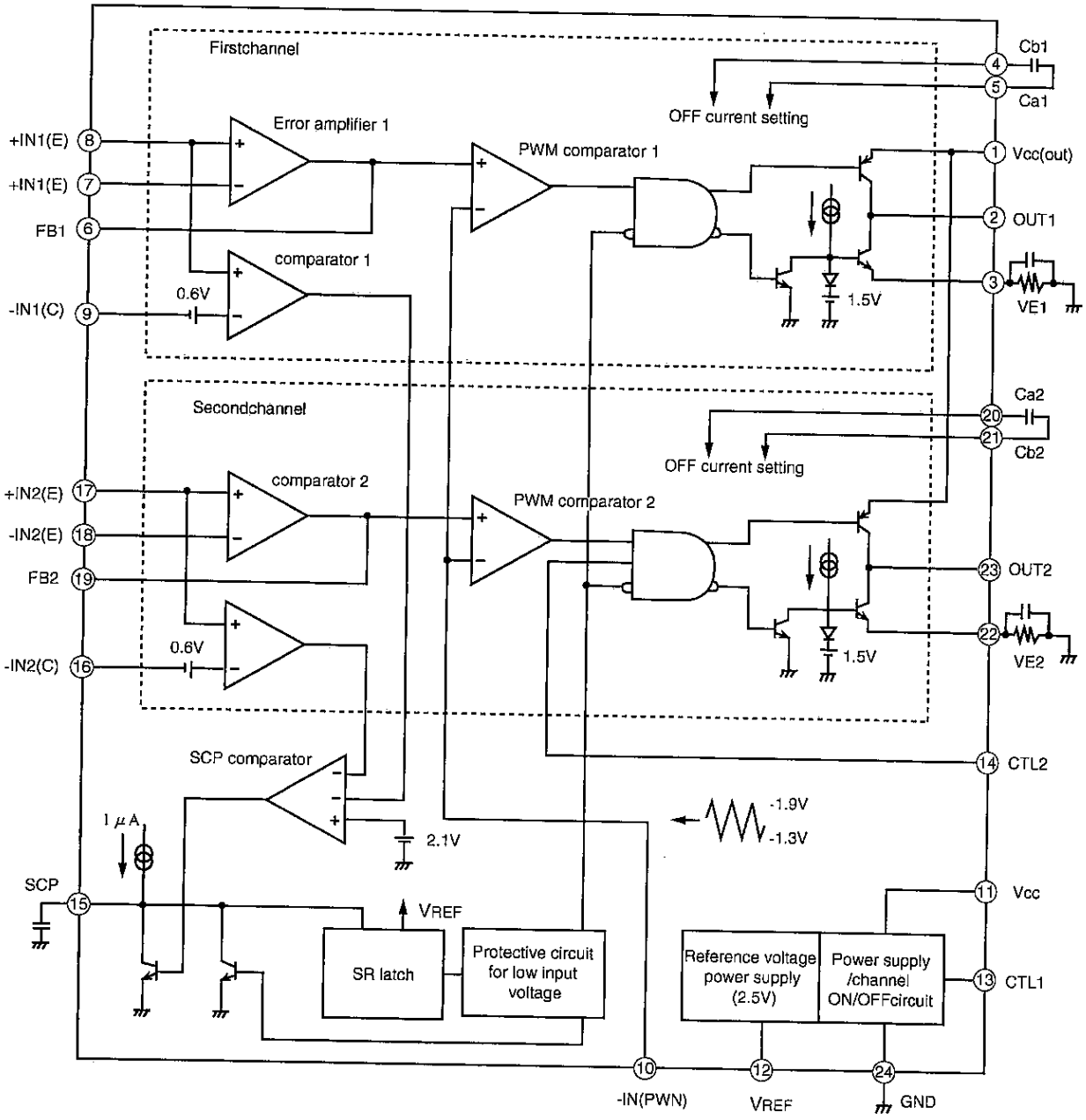


Note : The English letters parenthesized with ( ) at the terminal code show the input terminals of the next circuit.
(C): Comparator
(E): Error amplifier

■Terminal functions

Terminal No.		Terminal code	I/O	Terminal name and terminal function description
1st channel	2	OUT1	O	1st channel totempole type output terminal
	3	VE1	I	1st channel output current setting terminal
	5	Ca1	–	1st channel output transistor OFF current setting terminal Capacitor is connected between Cal terminal and Cb1 terminal to set the output transistor OFF current.
	4	Cb1	–	
	6	FB1	O	1st channel error amplifier output terminal
	7	–IN1(E)	I	1st channel error amplifier inverting input terminal
	8	+IN1(E)	I	1st channel error amplifier non-inverting input terminal
	9	–IN1(C)	I	1st channel error comparator inverting input terminal
2nd channel	16	–IN2(C)	I	2st channel error comparator inverting input terminal
	17	–IN2(E)	I	2st channel error amplifier non-inverting input terminal
	18	–IN2(E)	I	2st channel error amplifier inverting input terminal
	19	FB2	O	2st channel error amplifier output terminal
	20	Ca2	–	2st channel output transistor OFF current setting terminal Capacitor is connected between Cal terminal and Cb1 terminal to set the output transistor OFF current.
	21	Cb2	–	
	22	VE2	I	2st channel output current setting terminal
	23	OUT2	O	2st channel totempole type output terminal
Control circuit	13	CTL1	I	Power supply, 1st channel control terminal "H" level: Power supply, 1st channel is active. "L" level: Standby
	14	CTL2	I	2nd channel control terminal CTL1 terminal = "H" level "H" level: 2nd channel is active. "L" level: 2nd channel is off.
	15	SCP	–	Capacity connection terminal for short-circuit protection
Power circuit	1	V_{CC}(out)	–	Power terminal of output circuit
	10	–IN(PWM)	I	Oscillating waveform input terminal on the master side
	11	V_{CC}	–	Power terminal of reference power and control circuit
	12	V_{REF}	O	Reference voltage output terminal
	24	GND	–	Ground terminal

■Block diagram



■Functions

1. Switching regulator

(1) Reference voltage power supply circuit In the reference power circuit, the reference voltage (≒2.50V) which is compensated for the temperature by the voltage supplied from the power terminal (pin 11) is generated, and is used as the operational power supply of the inner circuit of IC.
Moreover, at the reference voltage, a maximum of 1 mA can be gained from V_{REF} (pin 12) to the external.

(2) Error amplifier

The error amplifier detects the output voltage of the switch regulator, and outputs the PWM control signal. The same-phase voltage range is as wide as -0.2V ~ Vcc-1.8V and can be easily set from the external power supply, thus being applicable for the DC motor speed control system and so on.
Moreover, since a desired loop gain can be set by connecting the feedback resistor and capacitor from the output terminal to the inverting input terminal of the error amplifier, the phase can be stably compensated.

(3) PWM comparator

The voltage comparator has the inverting input and non-inverting input, being the voltage-pulse width comparator which controls the on time of the output pulse according to the input voltage.
The master-side oscillated waveform which is input from the -IN(PWM) terminal turns on the output transistor while it is lower than the output voltage of the error amplifier.

(4) Output circuit

The output circuit is a structure of the totempole type which can drive a maximum of 30 mA with the PNP transistor drive system. (Refer to "n Setting method of output current".)

2. Channel control function

The channels are set on/off at the voltage levels of CTL1 terminal (pin 13) and CTL2 terminal (pin 14).

Table 1 On/off setting conditions of channels

<table>
<tr><td colspan="2">Voltage level of CTL terminal</td><td colspan="3">On/off state of channel</td></tr>
<tr><td>CTL1</td><td>CTL2</td><td>Power circuit</td><td>1st channel</td><td>2nd channel</td></tr>
<tr><td>L</td><td>X</td><td colspan="3">Standby state *</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td colspan="2" rowspan="2">ON</td><td>ON</td></tr>
<tr><td>L</td><td>OFF</td></tr>
</table>

* : The current value of the power in the standby state is 10μA or less.

3. Protective function

(1) Timer latch type short-circuit protective circuit

The SCP comparator detects the output voltage level of each comparator for short-circuit detection. If the output voltage level of any comparator becomes higher than 2.1V, the timer circuit will be activated to start charging the protection enable capacitor which is externally installed at the SCP terminal (pin 15).

If the output voltage level of the comparator does not return to the normal voltage level until the voltage of the capacitor rises to the base emitter junction voltage: VBE (≒0.65V) of the transistor, the latch circuit will be activated not only to turn off the output transistor but also to set the halt term at 100%. (Refer to "■ Time constant setting method of timer latch type short-circuit protective circuit".)

When the protective circuit is activated, it can be reset by turn on the power supply again.

(2) Malfunction-protective circuit for low input voltage

The transition state of the power turn-on and the instantaneous drop of the power voltage induces the malfunction of the control IC, thus destroying or degrading the system. The malfunction-protective circuit for low input voltage detects the inner reference voltage level according to the power voltage level, resets the latch circuit, turns off the output transistor, and sets the halt term at 100%, thus keeping the SCP terminal (pin 15) at the "L" level.

It will be returned if the voltage of the power supply becomes more than the threshold voltage of the malfunction-protective circuit for low input voltage.

■Outline view

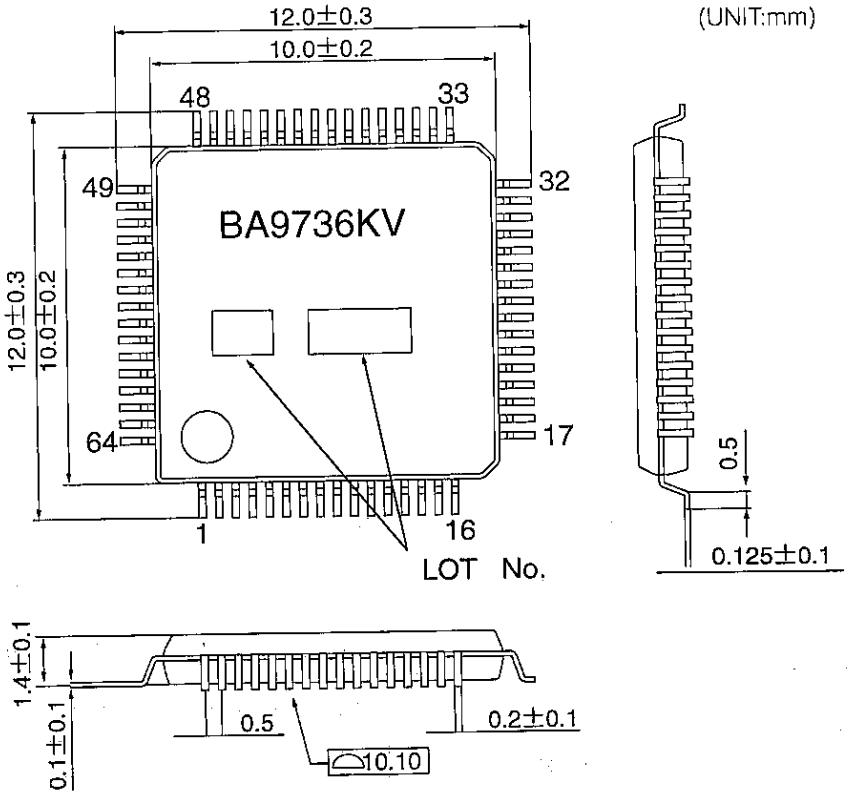


Figure 1.

■Terminal layout

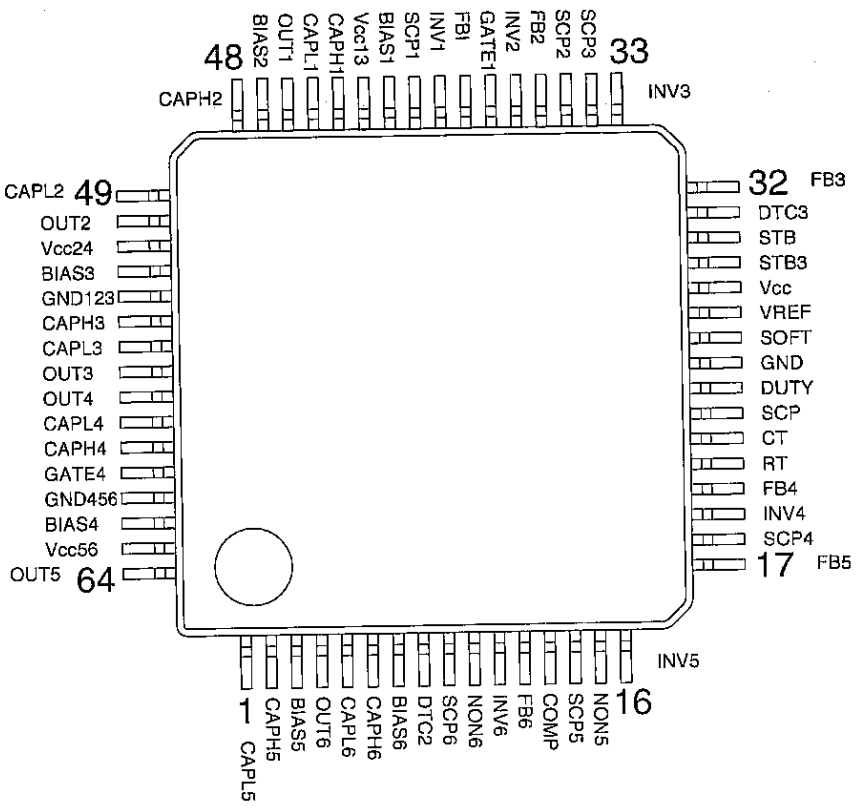


Figure 2.

■Terminal description

Terminal No.	Terminal name	Function
1, 5, 45, 49, 55, 58	CAPL 5, 6, 1, 2, 3, 4	Off transistor current setting capacitor connection L
2, 8, 44, 48, 54, 59	CAPH 5, 6, 1, 2, 3, 4	Off transistor current setting capacitor connection H
3, 7, 42, 47, 52, 62	BIAS 5, 1, 2, 3, 4, 5	Output current setting
4, 46, 50, 56, 57, 64	OUT 6, 1, 2, 3, 4, 5	Power transistor base connection
9, 14, 18, 34, 35, 41	SCP 6, 5, 1, 2, 3, 4	Output voltage monitor for CH1 thru CH6 holding
11, 16, 19, 33, 37, 40	INV 6, 5, 1, 2, 3, 4	Error amplifier inverting input
12, 17, 20, 32, 36, 39	FB 6, 5, 1, 2, 3, 4	Error amplifier output
13	COMP	Timer latch external trigger input
21	RT	Triangular timing resistor connection
22	CT	Triangular timing capacitor connection
23	SCP	Timer latch daisy setting capacitor connection
24	DUTY	MOSFET duty control
25	GND	Ground
26	SOFT	Soft start setting capacitor connection
27	VREF	Reference voltage output
28	VCC	Power supply input
29	STB3	CH3 ON/OFF switch
30	STB	All CH ON/OFF switch
8, 31	DTC 2, 3	Dead time control
36 , 60	GATE 1, 4	MOSFET gate connection
43	VCC13	CH1, CH3 output step power input
31	VCC24	CH2, CH4 output step power input
63	VCC56	CH2, CH6 output step power input
53	GND123	CH1, 2, 3 output step ground
61	GND456	CH4, 5, 6 output step ground
10 ,15	NON 6, 5	Error amplifier forward input

7. BLOCK DIAGRAM

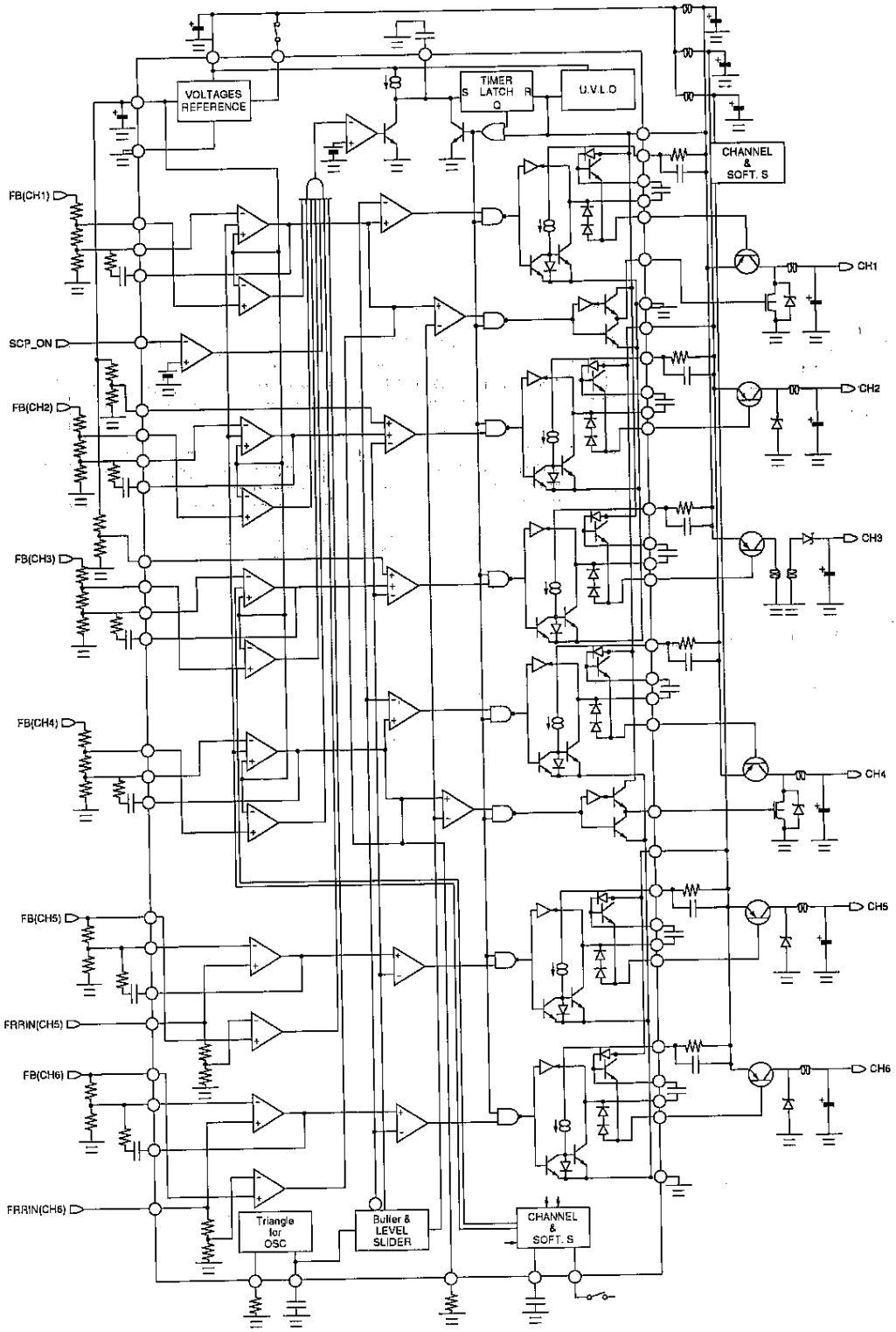


Figure 3.

UADP-0260TAZZ / UADP-0264TAZZ

Description of circuit operation

1. Operation description

The product is a charger for lithium ion battery which drives a camera-unitized 8 mm VCR, being composed of the fly-back type switching regulator as shown in Fig. 1.AC input is rectified with the input circuit unit once and is supplied to the primary circuit. The voltage is transferred through the transformer to the circuit unit on the primary side by repeatedly turning on and off the transistor at the pulse generating unit. Then, it is rectified by the rectifying unit on the primary side and is output to charge the battery. Here, AC input voltage variation and load variation are stabilized by the primary control unit and secondary control unit.
AC input is a world wide type of 100 to 240 V, 50/60 Hz.

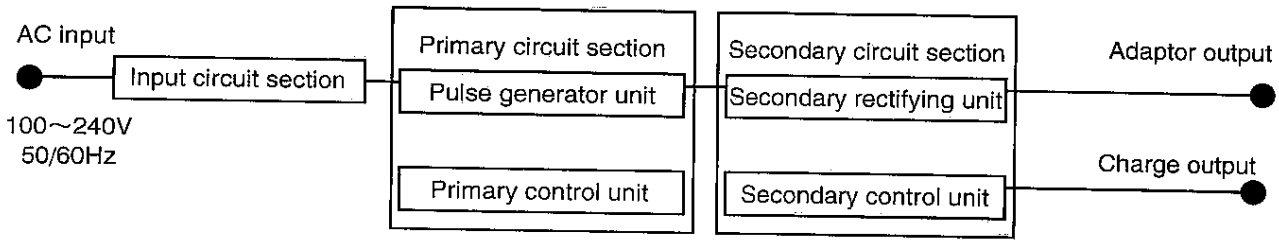


Fig. 1 Block diagram

2. VCR output operation

When the VCR output plug is connected to the charger, the output current is supplied to VCR to operate VCR.

3. Charging

When the lithium ion battery is installed on the charger, the charging current is supplied from the battery terminal to start charging.The following modes are provided for charging. The charging process is shown in Fig. 2.

(1) Preparatory charging mode

When the discharged battery is charged, approx. 60 mA is first preparatorily charged to the specified voltage (6.0 V).If the battery voltage does not reach the specified 6.0 V in 90 minutes, charging will be stopped.

(2) Rapid charging mode (pulse charge)

When the battery voltage becomes 6.0 V or more, the rapid charging mode will be selected and 1.4A will be charged in the pulse mode until the battery voltage reaches 8.6 V.
As the battery voltage rises, the charging current will be gradually reduced with the pulse width becoming larger.At the end of charging, variation of the battery voltage will be detected to stop charging. Otherwise, charging will be stopped by the timer of 150 minutes after start of charging.

4. Indication

LED (orange) indicates the charged state, and LED (red) indicates that power is supplied.

State	Charge LED	Power LED
Power OFF	Unlit.	Unlit.
Battery not installed	Unlit.	Lit.
Preparatory charging	Lit.	Lit.
Rapid charging	Lit.	Lit.
Charging completion	Unlit.	Lit.
Battery trouble • Shorted battery	Blinking	Lit.
Battery trouble • Overvoltage	Blinking	Lit.

5. Circuit description

According to the circuit diagram, the circuit of the charger is simply described.

(1) Input circuit section

AC input from the power line is smoothened at C2 through the rectifying diode D1, thus being converted into DC.The coil L1 and capacitor C1 work as a filter to reduce noise, and R1 and 2 are the resistor to discharge the charge remained at C2.

(2) Switching circuit on the primary side

The circuit repeatedly switches IC IC1 to generate the pulse voltage on the primary coil of the transformer T from the DC voltage generated in the input circuit section, thus inducing also the pluses in the secondary coil and primary coil of T1.D2, R73, C28 and L6 are the snubber circuit to prevent the surge voltage from generating in the primary coil of T1 when IC1 is turned off.
The signal is transferred to IC1 from the primary circuit section through the photo coupler PC1.The pulse signal whose width corresponds to the signal is output in IC1 and drives IC1. IC1 has the OVP circuit to stop output for excessive voltage, the circuit to limit the overcurrent, the soft start circuit for starting, the overheat protective circuit and other protective circuits.

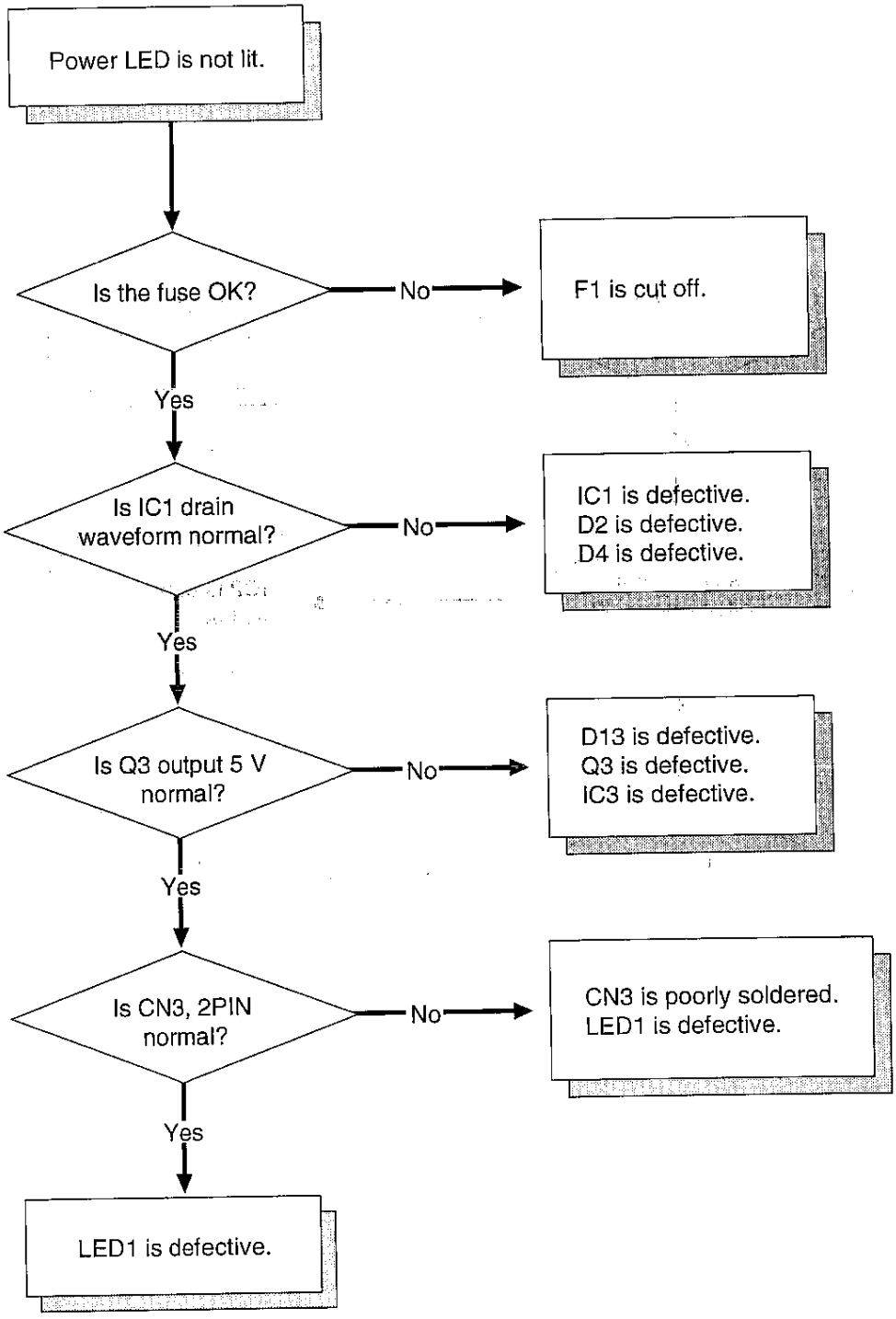
(3) Secondary circuit on the secondary side

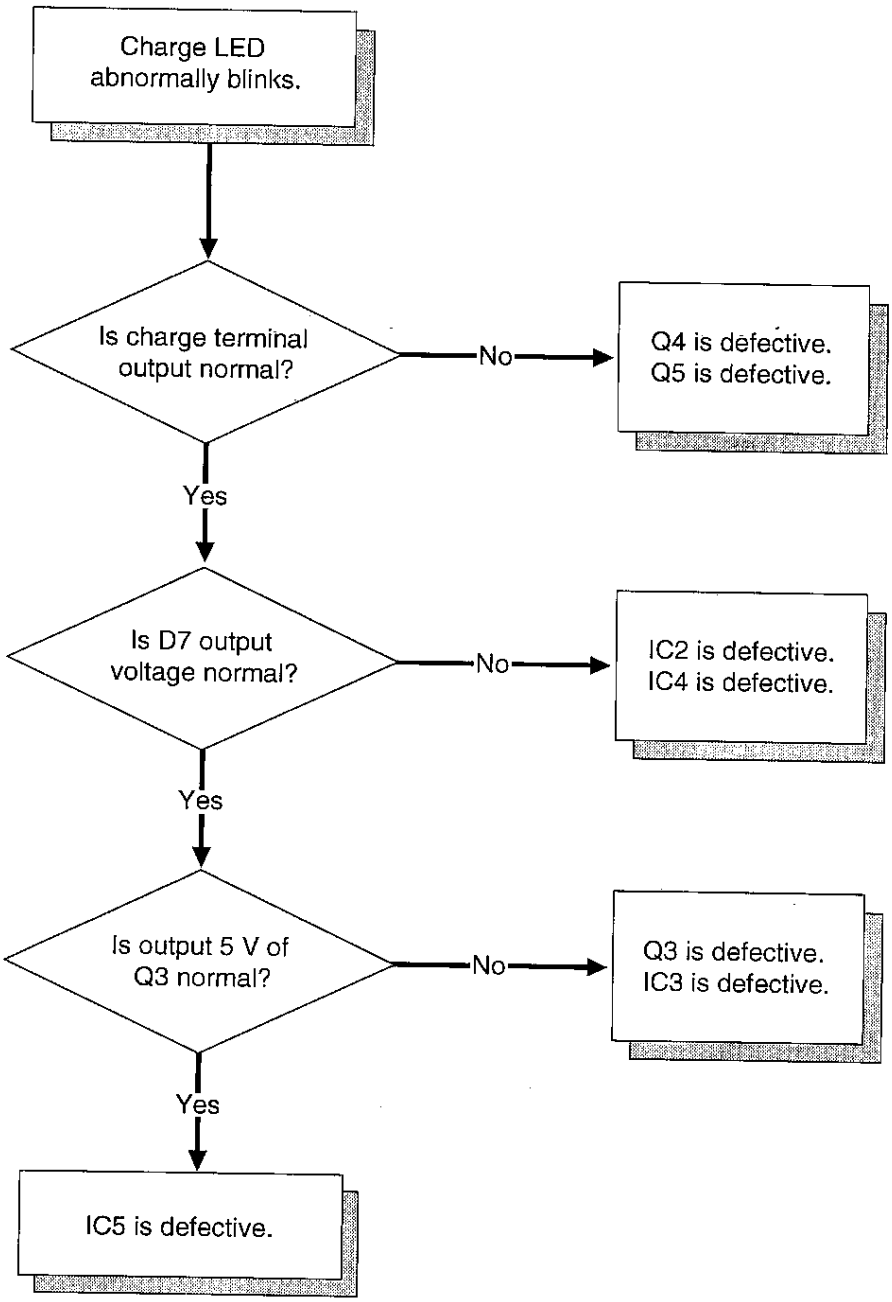
The pulse voltage generated in the secondary coil of T1 is smoothened with D7C12, L2 and C13, and becomes the DC stabilized output voltage. Moreover, the DC output rectified and smoothened by D13 and C32 becomes the power supply of the control section on the secondary side.
Q4 and Q5 are the transistors which switch on and off the charged current. When Q4 is on and Q5 is off, the preparatory charging is selected, and when Q4 and Q5 are off, rapid charging is selected.
Q8 is the transistor which switches on and off VCR output. When Q8 is on, VCR output is supplied.
IC2 has the control function for constant voltage and constant current. The output signal is fed back to the control section on the primary side through the photo coupler.
The constant current control section uses the detection resistor R59.
VR2 is used to adjust the charged voltage 8.6 V.
Q3 and IC3 are the 5 V constant voltage circuit to supply the reference voltage of the microcomputer IC5.
VR1 is used to adjust the 5 V constant voltage.The microcomputer IC5 detects the voltage of the battery to judge that charging is completed.

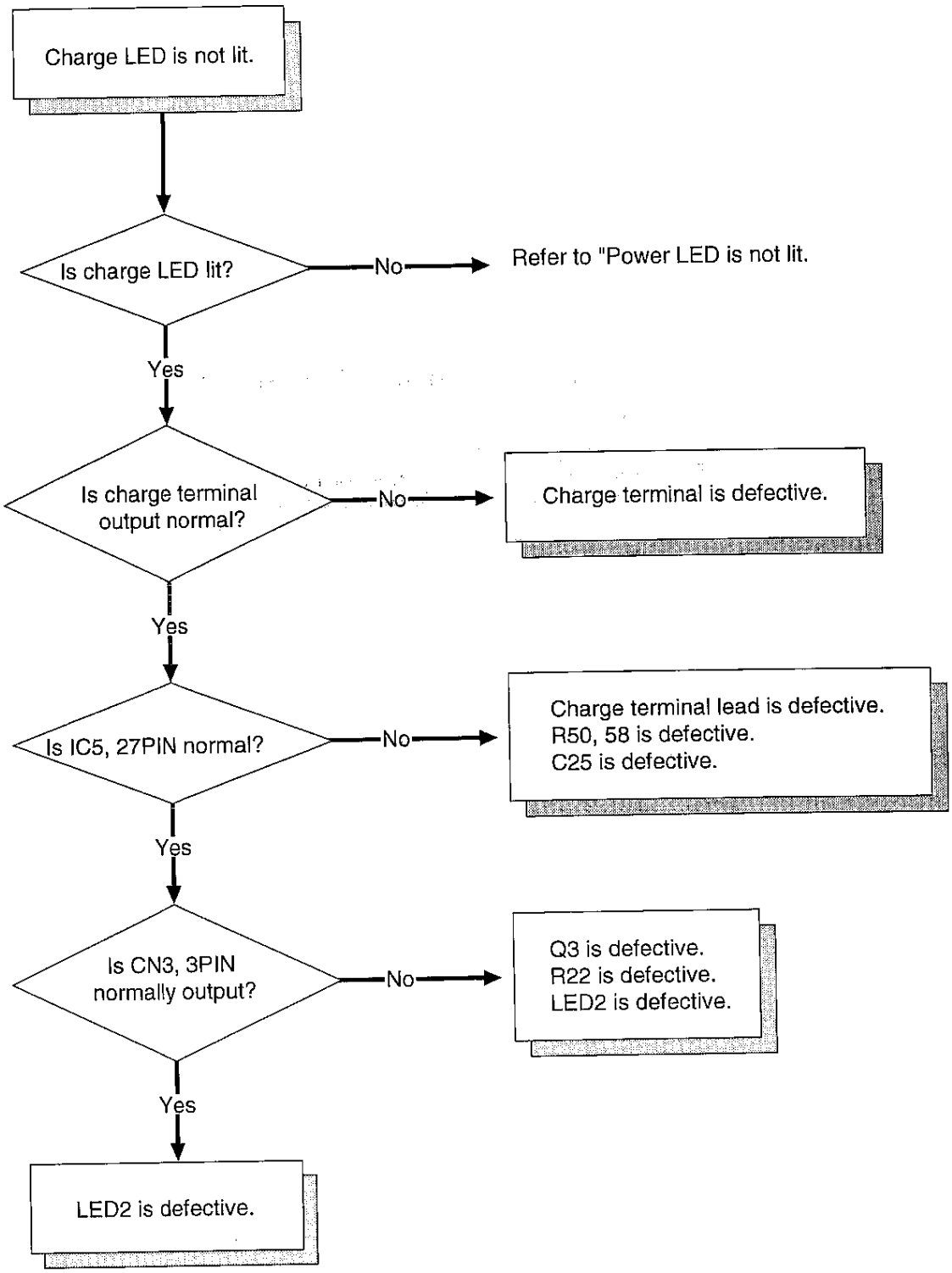
(4) Indication section

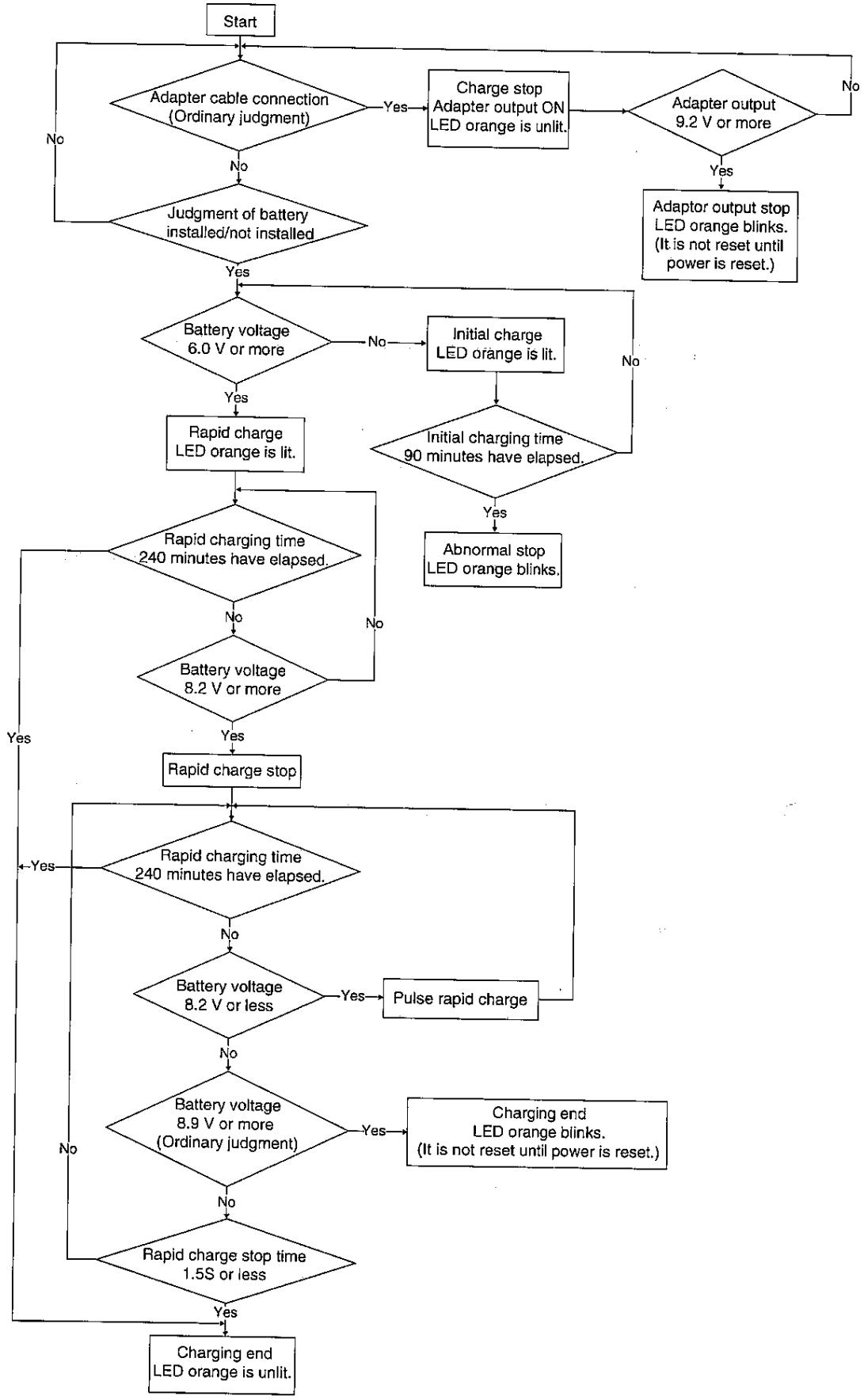
AC is energized to turn on LED1 (red).
LED2 indicates the charged state. LED2 (orange) is lit for preparatory charging and rapid charging and is unlit for completed charging. If the battery is troubled, LED2 (orange) will blink.

6. Troubleshooting




Charge LED abnormally blinks.
Is charge terminal output normal?
No
Q4 is defective.
Q5 is defective.
Yes
Is D7 output voltage normal?
No
IC2 is defective.
IC4 is defective.
Yes
Is output 5 V of Q3 normal?
No
Q3 is defective.
IC3 is defective.
Yes
IC5 is defective.


Charge LED is not lit.
Is charge LED lit?
No
Refer to "Power LED is not lit.
Yes
Is charge terminal output normal?
No
Charge terminal is defective.
Yes
Is IC5, 27PIN normal?
No
Charge terminal lead is defective.
R50, 58 is defective.
C25 is defective.
Yes
Is CN3, 3PIN normally output?
No
Q3 is defective.
R22 is defective.
LED2 is defective.
Yes
LED2 is defective.


Start
Adapter cable connection (Ordinary judgment)
Yes
Charge stop
Adapter output ON
LED orange is unlit.
Adapter output 9.2 V or more
No
Yes
Adaptor output stop
LED orange blinks.
(It is not reset until power is reset.)
No
Judgment of battery installed/not installed
Yes
Battery voltage 6.0 V or more
No
Initial charge
LED orange is lit.
No
Yes
Rapid charge
LED orange is lit.
Initial charging time 90 minutes have elapsed.
Yes
Abnormal stop
LED orange blinks.
Rapid charging time 240 minutes have elapsed.
No
No
Battery voltage 8.2 V or more
Yes
Yes
Rapid charge stop
Yes
Rapid charging time 240 minutes have elapsed.
No
Battery voltage 8.2 V or less
Yes
Pulse rapid charge
No
Battery voltage 8.9 V or more (Ordinary judgment)
Yes
Charging end
LED orange blinks.
(It is not reset until power is reset.)
No
No
Rapid charge stop time 1.5S or less
Yes
Charging end
LED orange is unlit.

8. MECHANICAL SECTION

Comparison Table of Digital Mechanism Service Parts

Screws and washers are excluded.

Drawing No	Part name / Model name		DH5000	DC1	DH4000 DC2/EX2	DX1	DC3 EX3	Remarks	Interchange-ability
300	Main chassis assembly	LCHSM****GEZZ	0156	→	→	0165	→	Brake latch lever shaft is abolished.	Old➡New
305	Tension arm assembly	MLEVF****GEZZ	0439 ➡0493.	0484	0493	0493	→	Others exceptDH500 are replaced with 0493.	Shown in the left
319	Mechanism fixture ANG-F	LANGJ****GEFW	0028	0030	→	0028	→	Shape is changed.	×
320	Mechanism fixture ANG-R	LANGJ****GE**	0029GEFW	0031GEZZ	→	0035GEFW	0036GEFW	Shape is changed.	×
322	Main cam	NGERH****GEZZ	3044	→	→	3048	→	The groove is reshaped due to abolishment of the brake solenoid.	×
323	Tu lock lever	MLEVE0482GESS	Yes	→	→	→	No	Because Tu lock mechanism is abolished.	×
324	Tu lock release lever	MLEVE0483GESS	Yes	→	→	→	No	Because Tu lock mechanism is abolished.	×
325	Cassette control stopper	LANGA0070GEFW	Yes	Yes➡No	No	→	→	The chassis hole is changed due to restriction of the upward stroke of the cassette control.	×
339	Tu guide catcher	LSTPP0001GEZZ	Yes	Yes➡No	No	→	→	DH5000 and DC1 can be abolished.	New⬅Old
341	Lock cam	PGIDM****GESS	0133	0151	→	→	→	Material change	Old⬅➡New
343	PWB holder Tu assembly	LHLDF1095GE**	1095GEZZ	→	→	→	1095GENZ	Tu lock lever installing shaft is abolished.	Old➡New
344	Brake latch lever	MLEVP0263GESS	Yes	→	→	No	→	Because brake solenoid is abolished.	×
345	Drum cover	PC0VP****GESS	1021	1022	→	1023	→	Shape is changed.	×
346	Tu reel retainer	LANGA0072GEFW	No	No➡Yes	No➡Yes	Yes	→	Individual addition is unnecessary. (Common for export model)	Old⬅➡New
352	Tu guide inner	NSFTL0725GEFW	Yes	No	→	→	→	Because Tu roller (414) is changed.	×
360	Brake latch lever spring	MSPRT0386GEFJ	Yes	→	→	No	→	Brake solenoid is abolished.	×
370	Tu lock spring	MSPRT0412GEFJ	Yes	→	→	→	No	Because Tu lock mechanism is abolished.	×
371	High-speed gear spring	MSPRP****GEFJ	0177	→	→	0168	→	Common with VSR gear spring (363).	×
396	Mechanism installing angle	LANGK0325TAFW	No	Yes	→	No	→		×
397	Floating rubber	PSPAG****TA00	0073	0077	→	No	→		×
398	Floating screw	LX-BZ****TA**	0189TAFD	0192TAFF	→	No	→		×
400	Mode SW-FPC	QPWBH****GEZZ	5206	→	→	5390	5206	Shape is change	×
413	SI roller assembly	NROL*****GESS	M0039	P0118	→	→	→	Material change	×
414	Tu roller	*********GE**	NPOLM 0041GEZZ	PGIDP 0028GEFW	→	→	→	Rotary roller➡Fixed post	×
431	Capstan motor	RMOTV****GEZZ	1017	→	→	1021	1017	FPC shape change	×
432	Brake solenoid	PRLu-008GEZZ	Yes	→	→	No	→		×
450	Sensor board assembly	CPWBN****GE01	5178	5346	→	5389	→	FPC shape change	×
462	Shield seat	PSLDM9091TAZZ	No	→	Yes	No	→	Noise countermeasure	×
501	Upper/lower drum complete assembly	0021HE**	01	02	03	04	→	Head, motor, FPC shape change DDRMW	×
507	Insulation tape	ZTAPEZ2111109M	No	→	→	Yes	No	Insulated from injection SW.	×
600	Cassette control complete assembly	CHLDX****GE01	3073 ➡3076	→	→	3079	→	DH5000 is superseded with 3076 (without black paint).	Shown in the left
701	Head amplifier board unit	RAMP-****TA**	0010TAN1	0015TAN0	→	0019TAN0	0020TAN0	Circuit, shape change	×
702	Head amplifier board angle	LANGT0455TAFW	Yes	No	→	→	→		×

SHARP

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